

MS-7636 Ver: 2.0 uATX(244mm X 210mm) 2010/5/19

CPU:

INTEL - Lynnfield/ Clarkdale LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH (H - 55)

OnBoard Chipset:

Clock Gen:ICS 4105B

Flash ROM: 64 Mb SPI (CHIP)

HD Audio Codec:VIA1818S

SIO:F71889ED

LAN:8131M 10/100/1000

USB 3.0 EJ168

SATA 6G JMB373

Main Memory:

DDRIII (800/1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Slot *1

PWM:

Controller: uP6206

(3-Phase use STD MOS -- 95W)

OV by uP6264 or SIO

uP6103 (CPU_VTT)

Linear (PCH)

uP6103(DDR)

GPU Power -ISL6314

ACPI: uPI+SIO

Other:

SATA(SATA2-300MB/s) *6

USB2.0 *10 (Rear*4 / Front*6)

PRINT Header *1

COM pin header *1

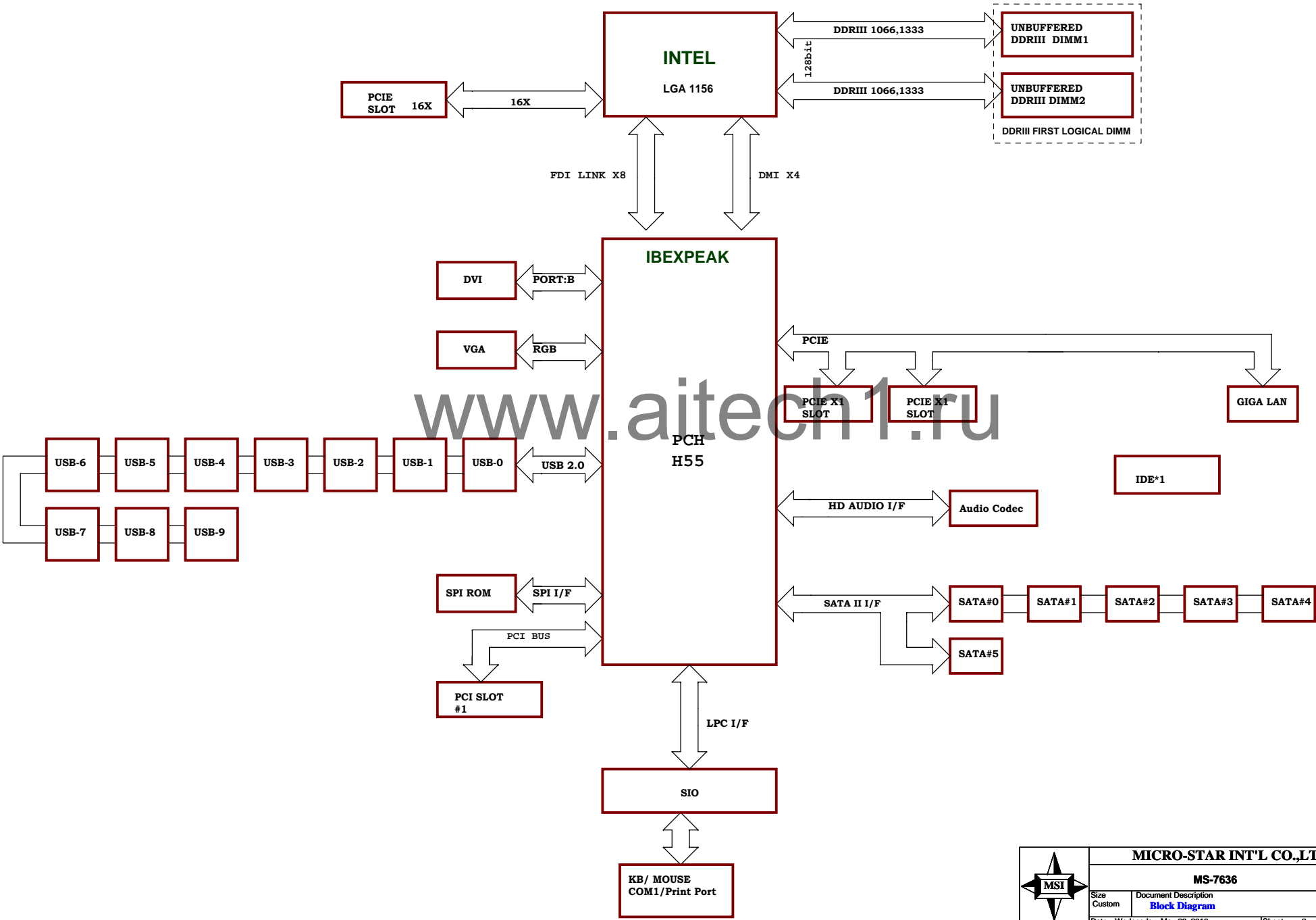
TPM Header *1

HDMI PORT*1

D-SUB *1

DVI PORT*1

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MS-7636		
Size Custom	Document Description Cover Sheet	Rev 2.0
Date: Wednesday, May 26, 2010 Sheet 1 of 40		



DDR DIMM config.

Device	Address	Clock
CHA DIMM1	10100001B	MEM_MA_CLK_H0/L0 H1/L1
CHB DIMM2	10100000B	MEM_MB_CLK_H0/L0 H1/L1

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D	PCI_REQ0# PCI_GNT0#	AD16	PCH CLKOUT_PCI<0>
TPM				PCH CLKOUT_PCI<3>
SIO				PCH CLKOUT_PCI<2>

TABLE 9↓
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #2	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#_PCH	PCISLOT1
PLTRST_BU2#	PCIE*16 / *1
PLTRST_BU3#	LAN&TPM
PLTRST#	SIO



MICRO-STAR INT'L CO.,LTD		
MS-7636		
Size Custom	Document Description Device Map	Rev 2.0
Date: Wednesday, May 26, 2010	Sheet 3	of 40

BEXPEAK GPIO DEFINITION									
Pin	GPIO	POWER WELL	I/O	Function	Implementation	Function			
AK41	GPIO0	MAIN	I	BMBSY#	Pull-up to +3.3V and connect to the PECL_REQ# pin (TBD) on the SIO	PECL_REQ#			
AL14	GPIO1	MAIN	I	TACH1	Through a 0.0 series resistor, connect to one of the front fan's TACH interface circuit.	TACH1			
AU8	GPIO2	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt E#			
AH7	GPIO3	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt F#			
AP12	GPIO4	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt G#			
AW4	GPIO5	MAIN	I	PCI_IRQ#	See PCA Spec	PCI Interrupt H#			
AY11	GPIO6	MAIN	I	TACH2	Pull-up to +3.3V and connect to P52-pin 12. The COMM_B assembly connects pin 12 directly to GND	COMM_B_DET#			
AY11	GPIO7	MAIN	I	TACH3	Through a 0.0 series resistor, connect to one of the front fan's TACH interface circuit.	TACH3			
AK30	GPIO8	RESUME	O	IO_C#	Reserved	Reserved			
AL28	GPIO9	RESUME	I	OC5	Associated with USB port 05 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#			
AL30	GPIO10	RESUME	I	OC6	Pull-up to +3.3VSB and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2			
AL31	GPIO11	RESUME	I	SMBALERT#	Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#			
AY34	GPIO12	RESUME	I	LAN_DISABLE	Follow implementation in Intel Piddon Design Guide	LAN_DISABLE#			
AR16	GPIO13	RESUME	I	IO_PME	Pull-up to +3.3V SB and connect to P151-pin 10; also add a no-installed pulldown to the net.	RDYBST_DET#			
AM30	GPIO14	RESUME	I	OC7	Pull-up to +3.3VSB and connect to the SMI pin on the SIO	DASH_SMI			
AY36	GPIO15	RESUME	I	POH_CP15	Reserved	SMW from SIO			
AM39	GPIO16	RESUME	O	SATAACP	Follow implementation in Intel Piddon Design Guide	Reserved			
AW11	GPIO17	MAIN	I	TACH0	Through a 0.0 series resistor, connect to one of the front fan's TACH interface circuit.	CPU_MISSED			
AM39	GPIO18	MAIN	I	PCI_CLKQ1#	Through a 1K series resistor, pull-up to +3.3V and connect to E15-pin 1.	TACH0			
AP38	GPIO19	MAIN	I	SATA1CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BOOT_BLK_REC#			
AP38	GPIO20	MAIN	I	PCI_CLKQ2#		BRD_ID1			
AT37	GPIO21	MAIN	I	SATA0CP	Pull-up to +3.3V and connect to P23-pin 4.	PCI_CLKRQ2#			
AN41	GPIO22	MAIN	I	SCLOCK	Pull-up to +3.3V and connect to P150-pin 10	FRNT_AUD_DET#			
AP14	GPIO23	MAIN	I	LDRQ1#	Pull-up to +3.3V and connect to the PCI SLOT Riser Detect circuit.	INT_USB_DET#			
AR34	GPIO24	RESUME	O	MEMLED	Through a 1k series resistor, pull-up to +3.3VSB and connect to P125-Pin 1	RISER_DET#			
AP33	GPIO25	RESUME	I	PCI_CLKQ3#		HOOD_SW_DET#			
AW37	GPIO26	RESUME	I	PCI_CLKQ4#		PCI_CLKRQ3#			
AP37	GPIO27	RESUME	O	OD_FLL_VREN		PCI_CLKRQ4#			
AY40	GPIO28	RESUME	O	POH_CP28		Reserved			
BA35	GPIO29	RESUME	O	SLP_LAN#	Connect to a circuit used to force the 3.3V_CL rail on.				
AT37	GPIO30	RESUME	I	SUS_PWR_ACK		WOL_EN			
AK40	GPIO31	MAIN	I	ACPRESENT	TBD. For now connect to a Test Point	ESATA_DET#			
AT40	GPIO32	MAIN	O	PCI_CP22	Through a 1k series resistor, pull-up to +3.3V and connect to P1-pin 20.	95%_RPS_DET#			
AT16	GPIO33	MAIN	O	PCI_CP23	Through a 1k series resistor, pull-up to +3.3V and connect to pin 1 of Jumper E1.	FDI_OVRD#			
AT40	GPIO34	MAIN	O	SP_PC#	Pull-down to GND and connect to: P124-pin 2, Decouple with 0.1µF	HOOD_LOCK_DET			
AK41	GPIO35	MAIN	O	SATACLKREQ#	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0			
AK39	GPIO36	MAIN	I	SATA2CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1			
AK38	GPIO37	MAIN	I	SATA3CP	Pull-up to +3.3V and connect to P125-pin 16	PRNTR_DET#			
AM38	GPIO38	MAIN	I	SL0AD	Through a series 1K resistor, connect to P5-pin 9 and pull-up to +3.3V	CHASSIS_ID0			
AL29	GPIO39	MAIN	I	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFR Basepan detect feature.	BASEPAN_DET#			
AT30	GPIO40	RESUME	I	OC1	Using an 8.2k resistor, pull-down to GND and connect to E40-pin 2	PASSWORD_EN			
AK28	GPIO41	RESUME	I	OC2	Associated with USB port 2 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#			
AP30	GPIO42	RESUME	I	OC3	Associated with USB port 3 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#			
AP31	GPIO43	RESUME	I	OC4	Associated with USB port 4 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#			
AP38	GPIO44	RESUME	I	PCI_CLKQ5#		PCI_CLKRQ5#			
AP36	GPIO45	RESUME	I	PCI_CLKQ6#		PCI_CLKRQ6#			
AP36	GPIO46	RESUME	I	PCI_CLKQ7#		PCI_CLKRQ7#			
AY39	GPIO47	RESUME	I	PEG_A_CLKRQ#		PEG_A_CLKRQ#			
AG38	GPIO48	MAIN	I	SDATAOUT1	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET#			
AG40	GPIO49	MAIN	O	SATA3CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0			
AW5	GPIO50	MAIN	I	PCI_REQ#1	Use as REQ1#.	REQ1#			
AK6	GPIO51	MAIN	O	PCI_GNT1#	Use as GNT1#.	GNT1#			
AT4	GPIO52	MAIN	I	PCI_REQ#2	Pull-up to +3.3V	REQ2#			
BA9	GPIO53	MAIN	O	PCI_GNT#2	Connect to TP	GNT2#			
AM3	GPIO54	MAIN	I	PCI_REQ#3	Through a 8.2K series resistor, connect to P14-pin 2 and pull-down to GND.	BOOT_BLK_EN#			
AM3	GPIO55	MAIN	O	PCI_GNT#3		GNT3#			
AW35	GPIO56	RESUME	I	PEG_B_CLKRQ#	Connect to circuit that controls the amplifiers output.	AUD_AMP_DIS#			
AL32	GPIO57	MAIN	I	POH_CP57	Pull-up to +3.3VSB.	TPM_PP			
AY31	GPIO58	RESUME	O	SML1CLK		SML1CLK			
BA37	GPIO60	RESUME	O	SMBALERT#		SMBALARM			
AK31	GPIO61	RESUME	O	SUS_STAT#	Power Down for external TPM	LPICP#			
AM31	GPIO62	RESUME	O	SUSCLK	SUSCLK to SIO	SUSCLK			
AD36	GPIO63	RESUME	O	SLP_S#	Connect to USB Power Control on SIO	SLP_S#			
AD10	GPIO64	MAIN	O	CLKOUTFLEX0		CLKOUTFLEX0			
AK1	GPIO65	MAIN	O	CLKOUTFLEX1		CLKOUTFLEX1			
AK6	GPIO66	MAIN	O	CLKOUTFLEX2		CLKOUTFLEX2			
AL3	GPIO67	MAIN	O	CLKOUTFLEX3		CLKOUTFLEX3			
AT34	GPIO72	RESUME	I	POH_CP72	Through a series 1K resistor, pull-up to +3.3VSB and connect to P5-pin 10.	CHASSIS_ID1			
AN35	GPIO73	RESUME	I	PCI_CLKRQ0#		PCI_CLKRQ0#			
AY32	GPIO74	RESUME	O	SML1ALERT#		SML1ALERT#			
AR31	GPIO75	RESUME	O	SML1DATA		SML1DATA			

SIO9 PIN ASSIGNMENT (UPDATE PENDING)			
Pin	Pin Name	Function	Implementation
1	PWRBTN#	PWRBTN#	Connect to front panel header's power button pin
2	SLP_S3#	SLP_S3#	Connect to ICH10's SLP_S3# signal
3	SLP_S5#	S4_STATE#	Connect to ICH10's S4_STATE# signal
7	PDS_EN	CPU_FAN_TACH	Connect to the CPU fan tach interface
8	COLOR	LED_PWR_COLOR	Controls the Power LED color
10	PWBTOUT#	PWRBTN_OUT#	Connect to ICH PWRBTN# input
11	PS_ON#	PS_ON#	Connect to the appropriate power supply circuit
13	BLINK_GR	LED_PWR_BLINK	Connect to PS.2 through 68 ohm series resistor.
14	SIOPME#	RING#	Connect to ICH8 R#
17	CLAMP_CTRL	CLAMP_CNTL	Use for clamping PCA voltage rails to decrease rail decay time
28	SMBISCL	SMB_CLK_MAIN	Connect to the clock signal of the main powered system SMBus
29	SMB2SCL	SMB_CLK_STDBY	Connect to the clock signal of the standby powered system SMBus
33	GPRST2#	PCI_EXP_RST#	Use to reset all the PCIe devices and slots
34	FANPWM2	CHAS_FAN_PWM	Connect to the Chassis Fan PWM interface
35	GPIO25	PWM_IN	Connect to the ICH10's PWM0 output - NEW for Eaglelake
36	PME_IN#	P_PME#	Connect to the PME# pin of the ICH10
37	USB_PWR#	USB_PWR#	Input to USB Power control; connect to the ICH10's SLP_S5# signal
38	3V_SW_MAIN#	3V_DUAL_CNTL	Connect to control inputs of dual rail switches
39	EVENT6#	PCI_EXP_WAKE#	Connect to WAKE# pins of PCIe devices and slots
47	PDS_EN2	PDS_EN2	Use as control signal for appropriate voltage regulators
48	CPU_PRSNT1#	SKTOCC#	Connect to SKTOCC# on CPU
49	WAKE_OUT#	ICH_WAKE#	Connect to the ICH10's WAKE# input
50	GPIO14	HOOD_LOCK#	Connect to P124 pin 1 and a 2.2K pull-up to +5V.
51	GPIO16	HOOD_UNLOCK#	Connect to P124 pin 6 and a 2.2K pull-up to +5V.
53	AUDIO_BEEP	DIAG_BEEP	Connect to the system's integrated audio solution
54	FANPWM1	CPU_FAN_PWM	Connect to the CPU fan's PWM circuit
55	GPIO35	PECL_REQ#	Connect to the ICH10's BM_BUSY# signal - New for Eaglelake; C#C4 support
56	HD_LED_IN#	SATA_LED#	Connect to the ICH10's SATA_LED# output signal
58	HMSCL	HLTH_MON_CLK	Connect to CLK pin on SensorBus device
59	HMSDA	HLTH_MON_DAT	Connect to DAT pin on SensorBus device
60	GPIO10	FLPY_DRV DEN	Use in floppy implementation
61	HD_LED_OUT#	HD_LED#	Connect to the front panel HDD LED
100	SMB1SDA	SMB_DATA_MAIN	Connect to the data signal of the main powered system SMBus
101	SMB2SDA	SMB_DATA_STDBY	Connect to the data signal of the standby powered system SMBus
102	5V_USB_MAIN	5V_USB_MAIN#	Connect to the control pin of the 5V_DUAL circuit.
103	GPIO41	PS_FAN_TACH	Where applicable, connect to power supply's fan tach circuit.
104	FANPWM3	PS_FAN_PWM	Where applicable, connect to the power supply's fan PWM circuit
105	PWRGD_01	PWRGD_30MS#	Use for appropriate system board sequencing
106	PWRGD_02#	PWRGD_30MS#	Use for appropriate system board sequencing
110	FAN_TACH4	CHAS_FAN_TACH	For systems with a chassis fan, connect to the chassis fan TACH circuit
111	SM1#	LPC_SM1#	Connect to appropriate ICH10 SMI-capable GPIO, reference ICH10 GPIO matrix
120	R12#	R12#	Where applicable, connect to appropriate serial port pin
122	DCD2#	DCD2#	Where applicable, connect to appropriate serial port pin
123	SIN2	SIN2	Where applicable, connect to appropriate serial port pin
124	SOUT2	SOUT2	Where applicable, connect to appropriate serial port pin
125	DSR2#	DSR2#	Where applicable, connect to appropriate serial port pin
126	RTS2#	RTS2#	Where applicable, connect to appropriate serial port pin
127	CTS2#	CTS2#	Where applicable, connect to appropriate serial port pin
128	DTR_BOUT2#	DTR2#	Where applicable, connect to appropriate serial port pin



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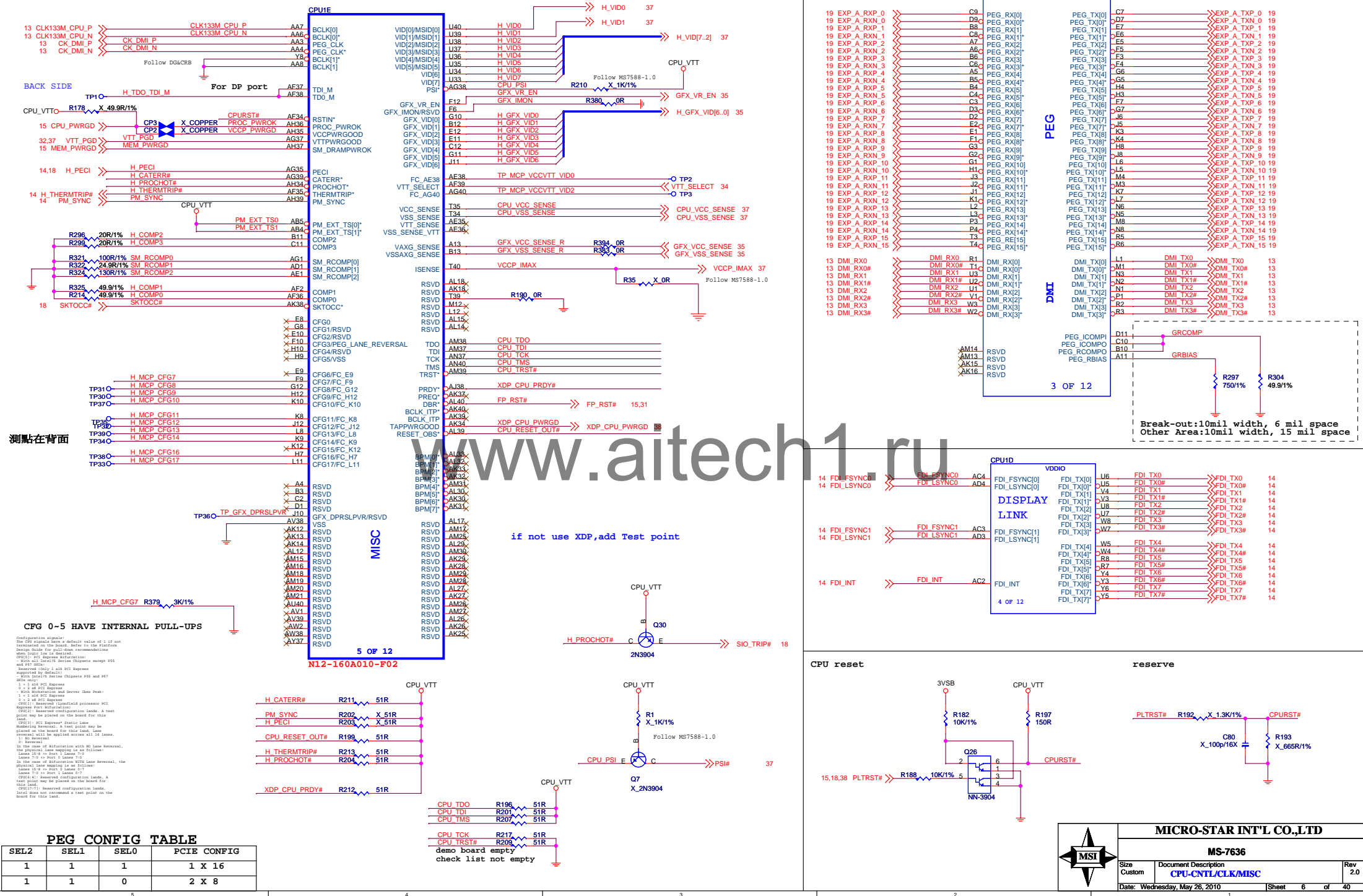
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	GPIO Table	
Date: Wednesday, May 26, 2010	Sheet 4 of 40	

History


- 1.2009-10-13 Change VCC_SENSE to CPU_VCC_SENSE
- 2.2009-10-13 Add HDMI circuit,change USB circuit,JSP1 circuit update
- 3.2009-10-13 update NCT3016 circuit ,add VTIN3 circuit for VRM MOS
- 4.2009-10-18 Add C589 C590
- 5.2009-10-18 Add R561 R562 For HDMI HPDET
- 6.2009-10-20 Add R602,Swap HDMI wire for layout
- 7.2009-10-21 NCT3016 circuit update:add R637 Q65 R592,Change U27 pin16 tp NCT_GPIO16,delete C121
- 8.2009-10-21A NCT3016 citcui update:add Q85,chang SATA1&SATA2 to SATA1_2
- 9.2009-10-23 change JUSB2 & JUSB1 for layout
- 10.2009-10-23A NCT3016 circuit update:add R850
- 11.2009-10-24 delete VCCGATE and DUALGATE circuit
- 12.2009-10-26 delete C534
- 13.2009-10-26 Swap RN40

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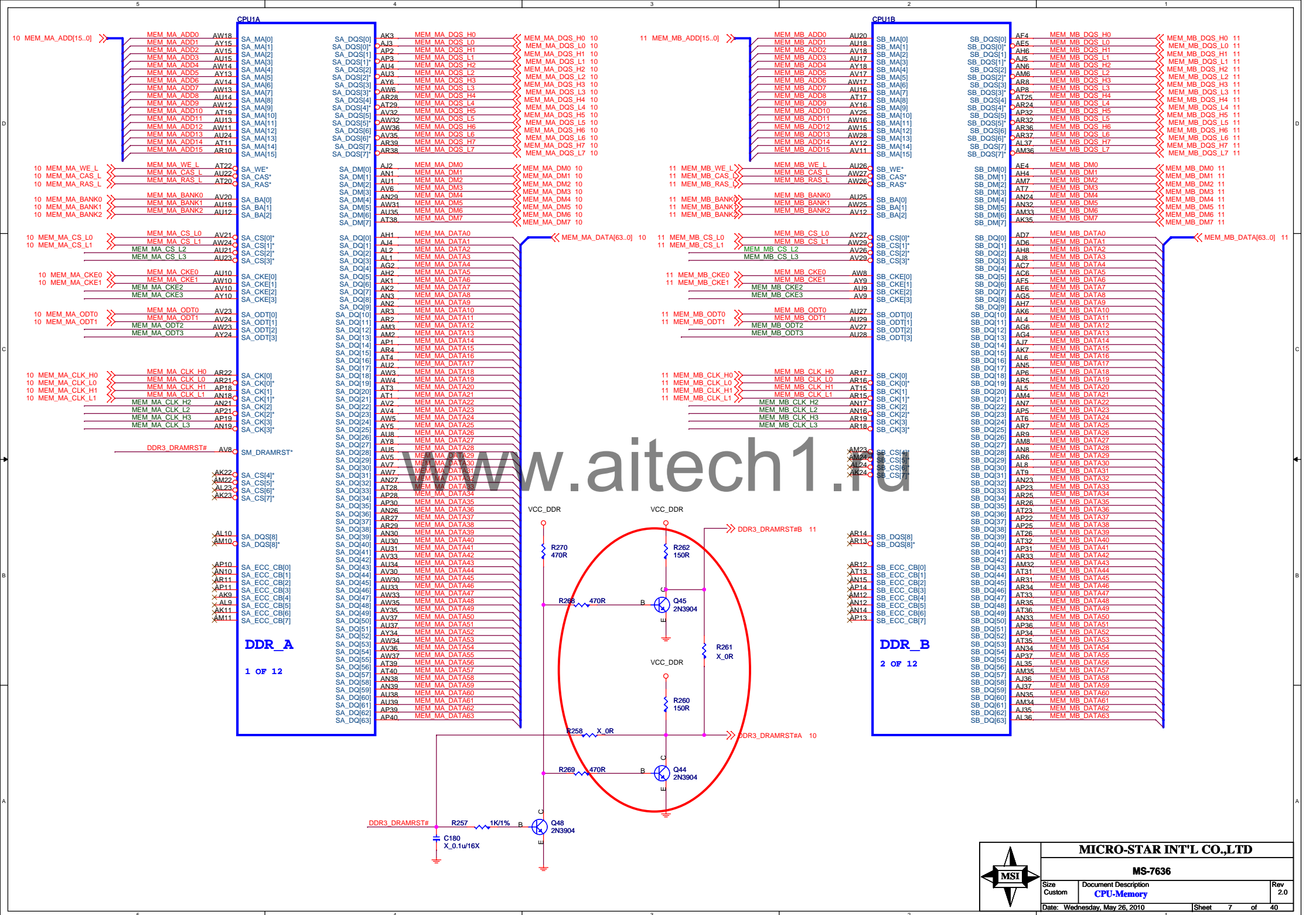
AAB/Y8 :these signals for 120 MHz from the Intel CPU_P / CLKOUT_DP_P / CLKOUT_DP_N / CLKOUT_BCLK1_P and CLKOUT_BCLK1_N. Leave as NC on the PCH and connect directly to GND at the processor. 120MHz clock is used for embedded DisplayPort which is no supported on Desktop designs.

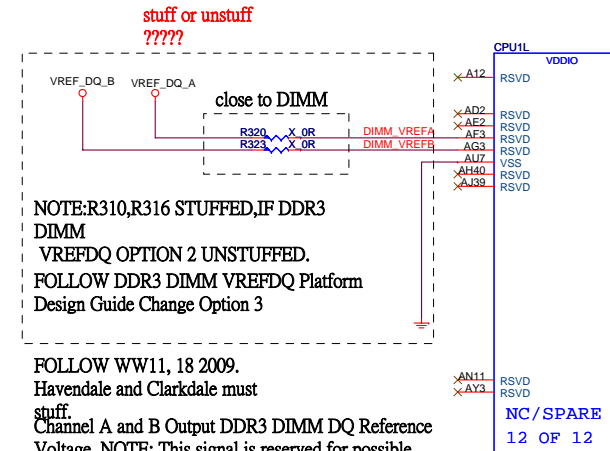
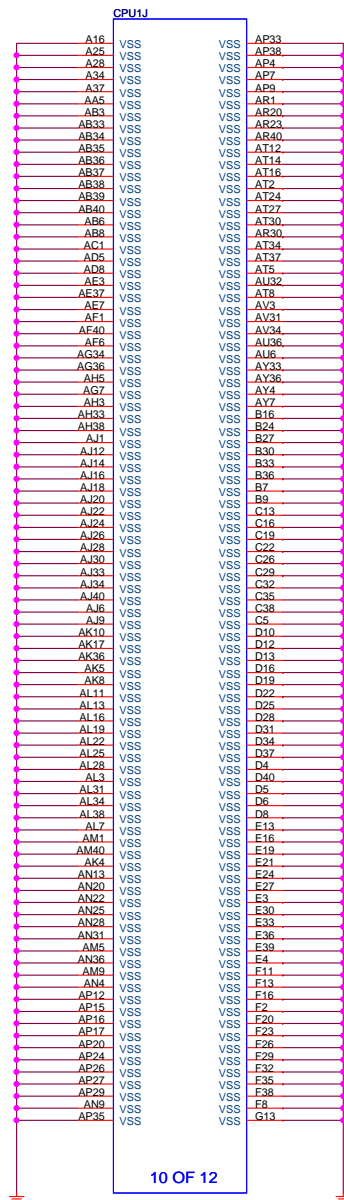


PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
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1	1	0	2 X 8

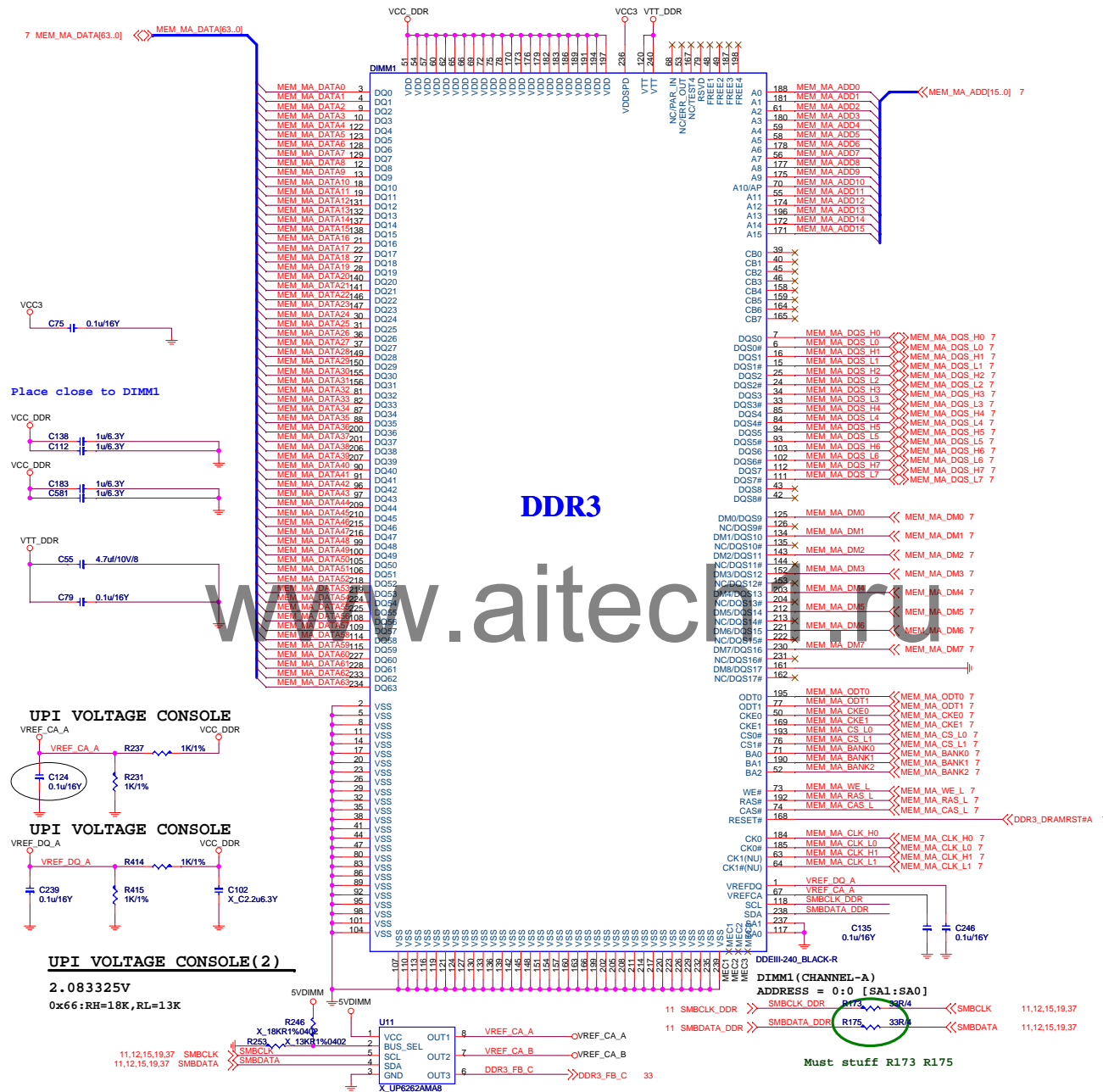


MICRO-STAR INT'L CO.,LTD		
MS-7636		
Size Custom	Document Description CPU-CTL/CLK/MISC	Rev 2.0
Date: Wednesday, May 26, 2010	Sheet 6	of 40





DDRIII DIMM_A1

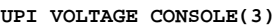



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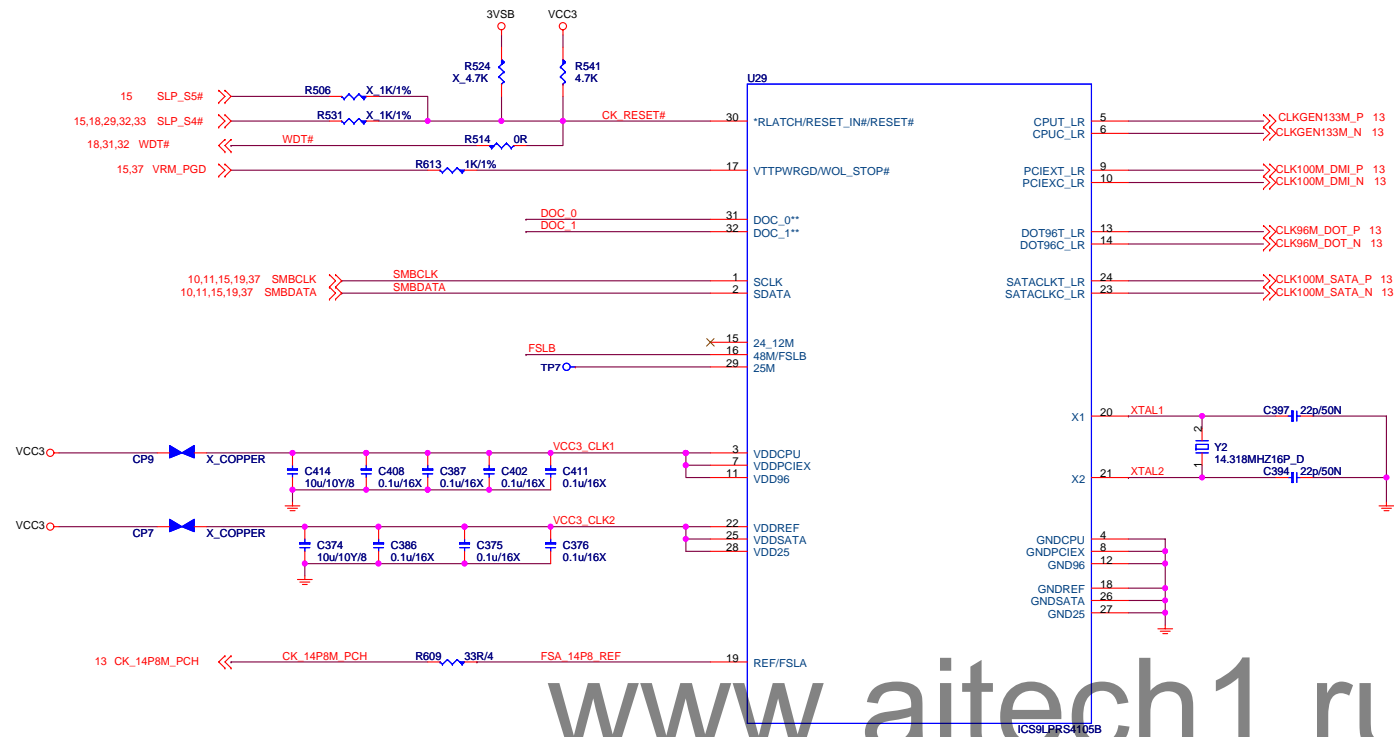
MS-7636

Size Custom	Document Description DDR3 Chanel-A DIMM1/2	Rev 2.0
Date: Wednesday, May 26, 2010		Sheet 10 of 40

DDR3



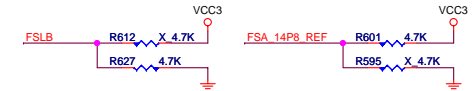
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	MS-7636		
	Size Custom	Document Description DDR3 Chanel-B DIMM3/4	Rev 2.0
	Date: Wednesday, May 26, 2010		Sheet 11 of 40



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CLOCK GEN STRAPING

FS4	FS3	FS2	FSB	FSA	CPU	Spread
80b4	80b3	80b2	80b1	80b0	Mhz	%
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5

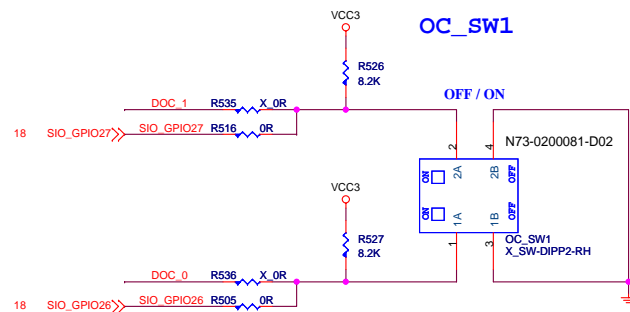


Pin16: 48MHz clock output. / 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values.

Pin19: 14.318 MHz reference clock. / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.

OC

DOC_0*:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.

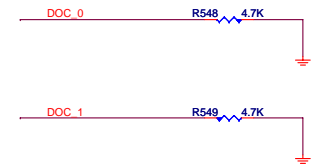
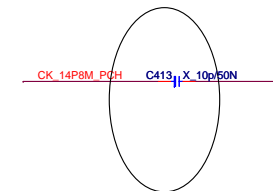


OFF=1 ; ON=0

DOC	TABLE
1 0	CPU FREQUENCY
1 1	133 MHz (default)
1 0	142 MHz
0 1	150 MHz
0 0	166 MHz

(Default) OFF / OFF
OFF / ON
ON / OFF
ON / ON

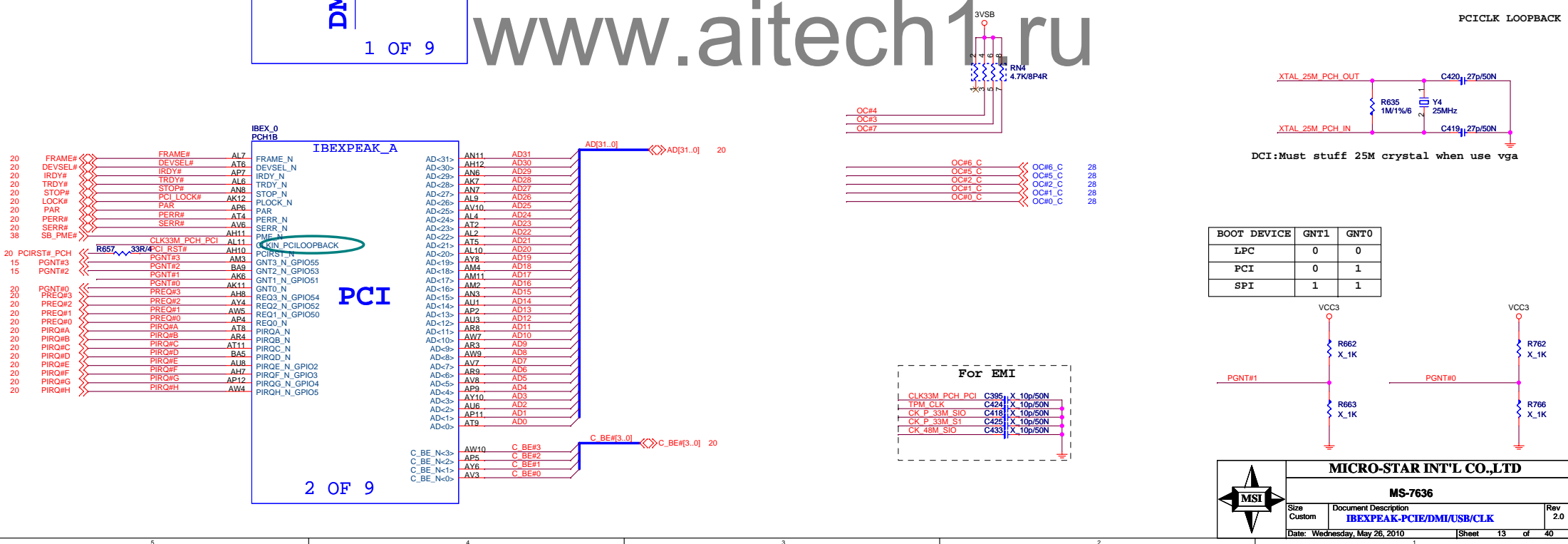
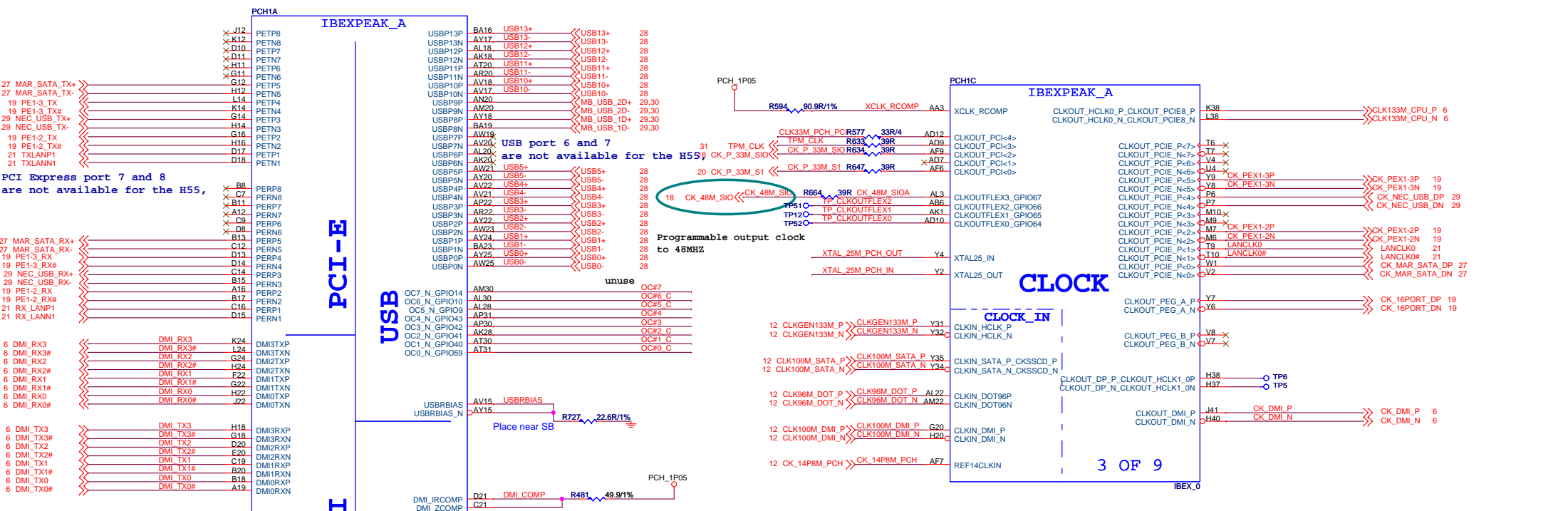
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MS-7636

Size	Document Description	Rev
Custom	CLK IC9LRS41058	2.0
Date: Wednesday, May 26, 2010	Sheet 12 of 40	



PCICLK LOOPBACK

DCI: Must stuff 25M crystal when use vga

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

VCC3

PGNT#1

PGNT#0

MSI

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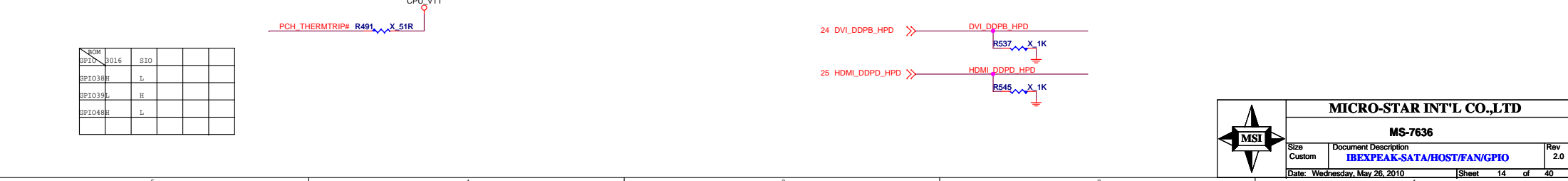
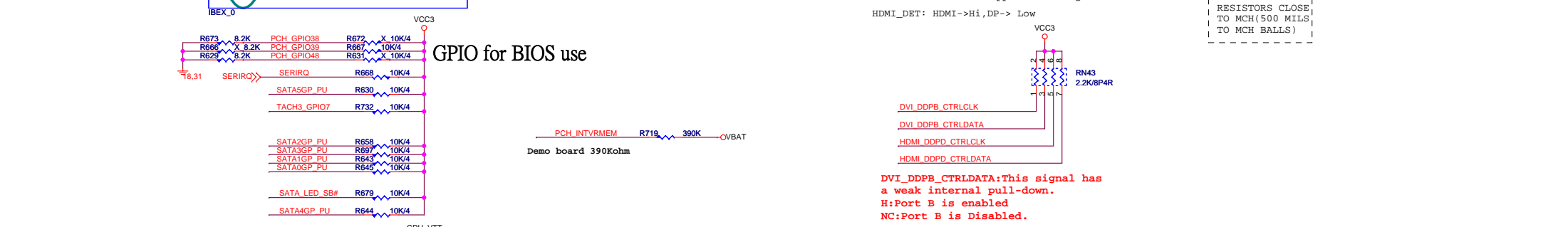
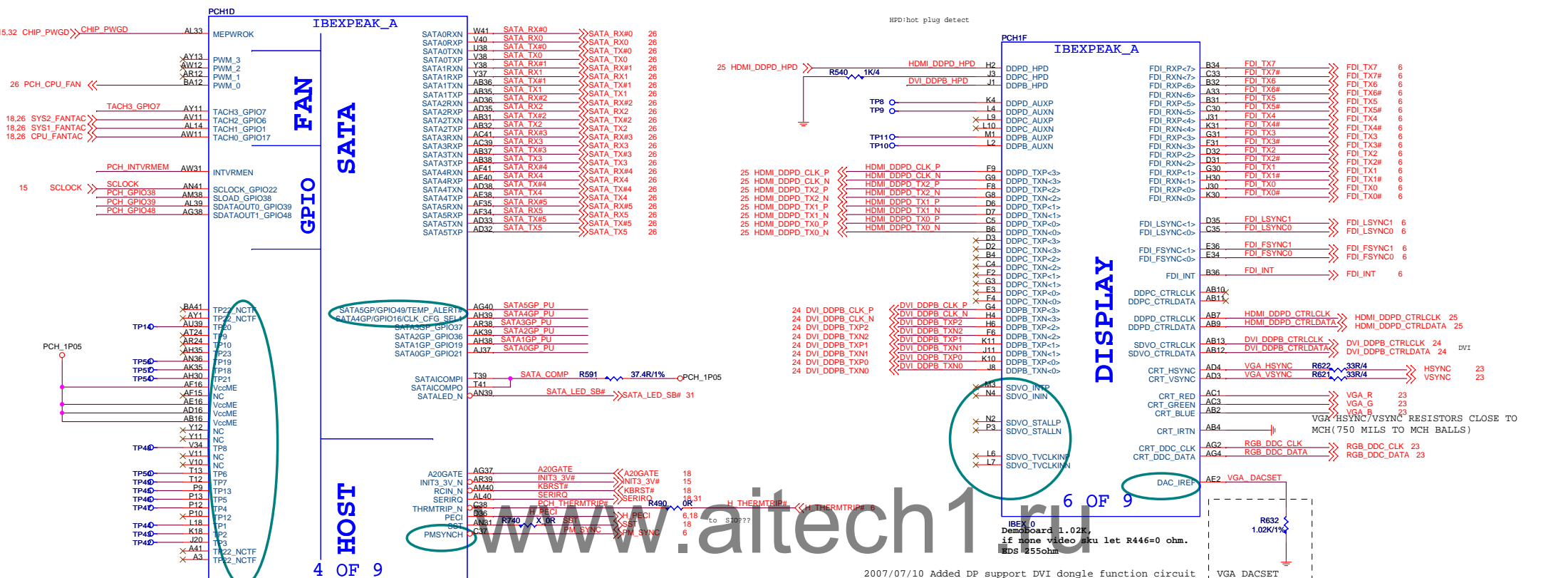
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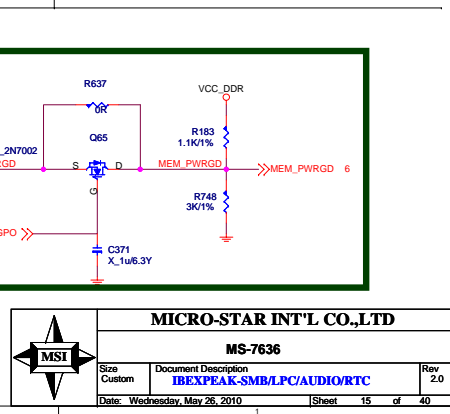
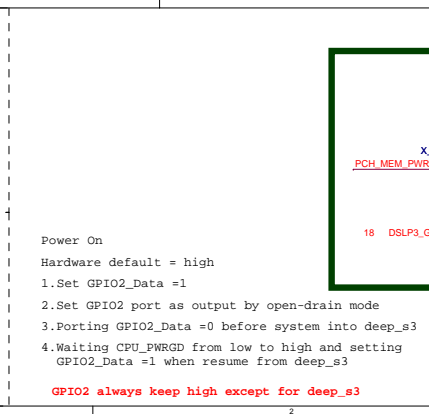
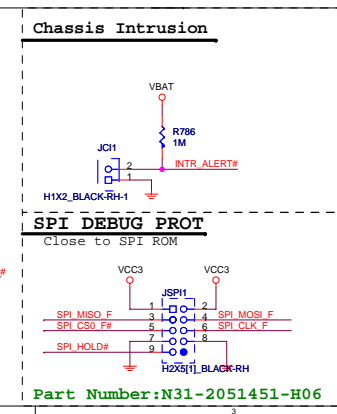
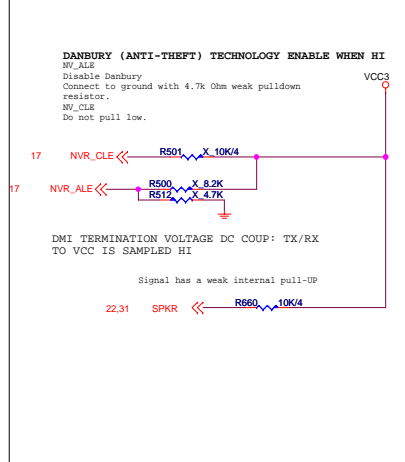
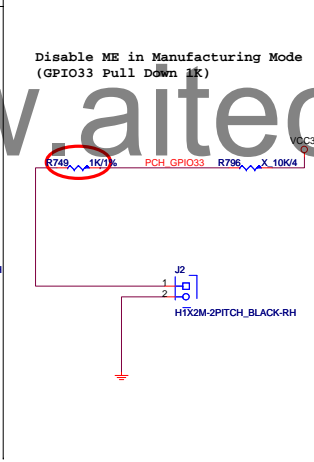
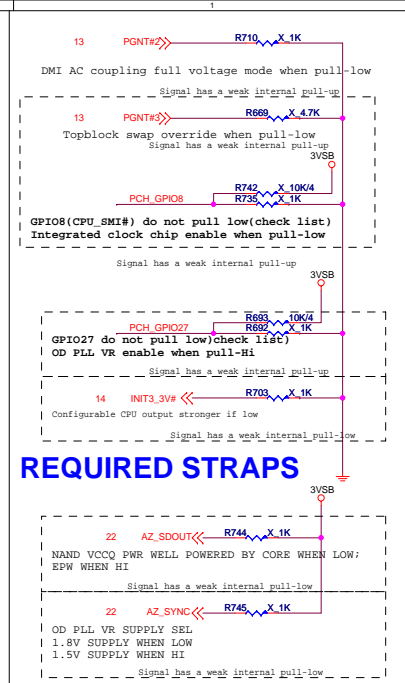
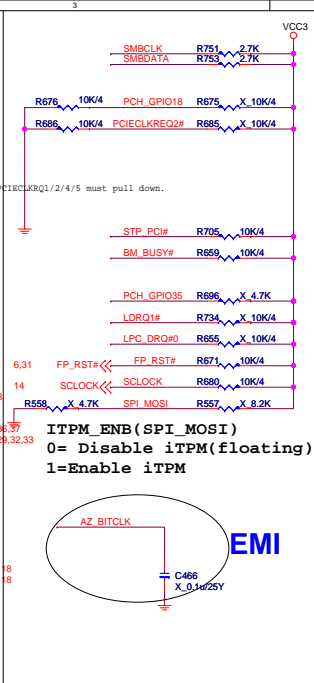
IBEXPEAK-PCIE/DMI/USB/CLK

Date: Wednesday, May 26, 2010

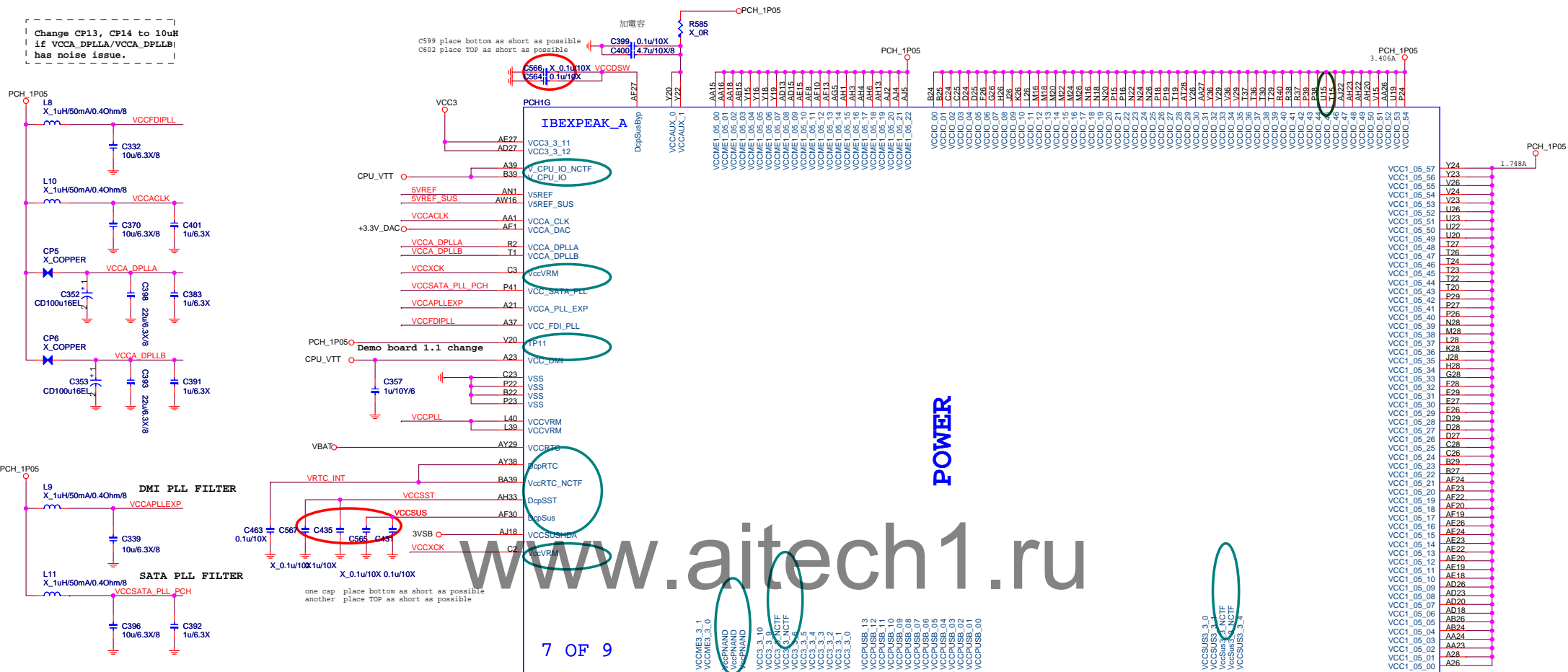
Sheet 13 of 40

Rev 2.0





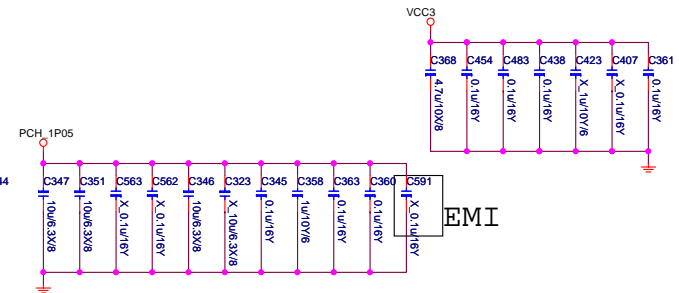
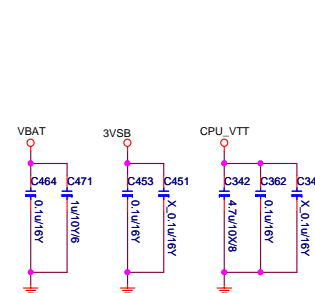
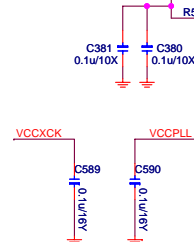
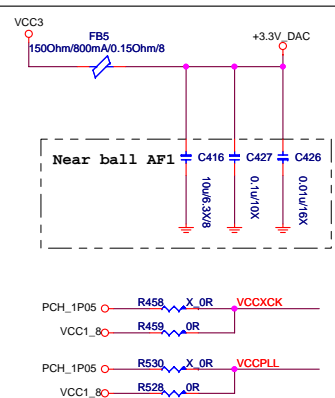
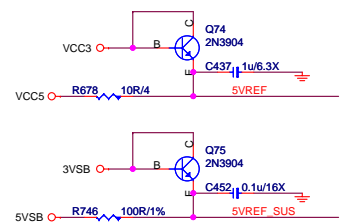

```
| Change CP13, CP14 to 10uH
| if VCCA_DPLLA/VCCA_DPLLB
| has noise issue.
```



PCH decoupling cap

5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.

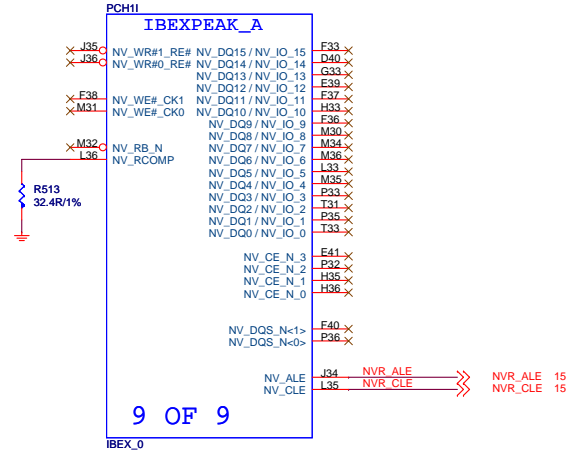
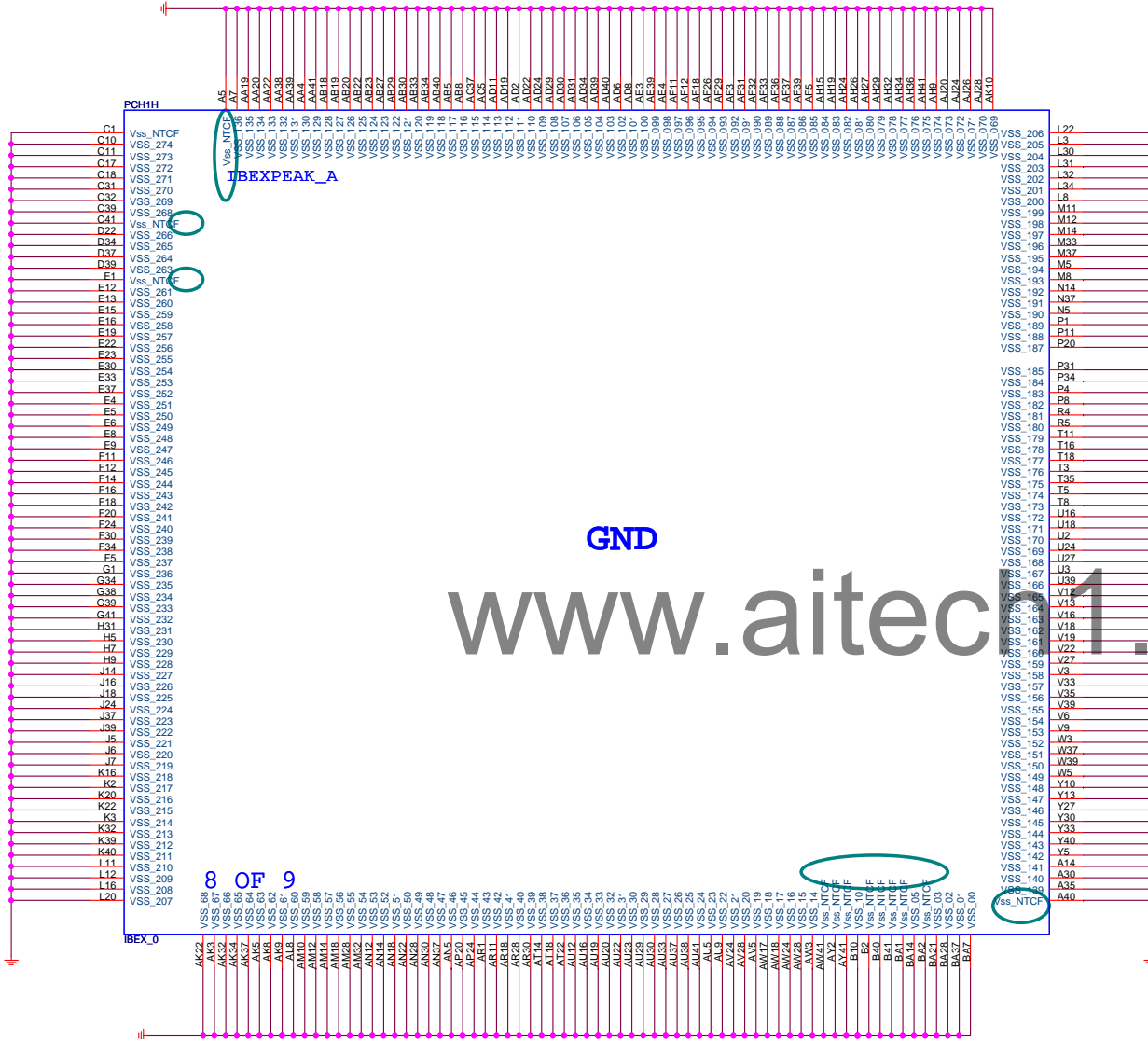


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MS-7636

Size Custom	Document Description IBEXPEAK-POWER
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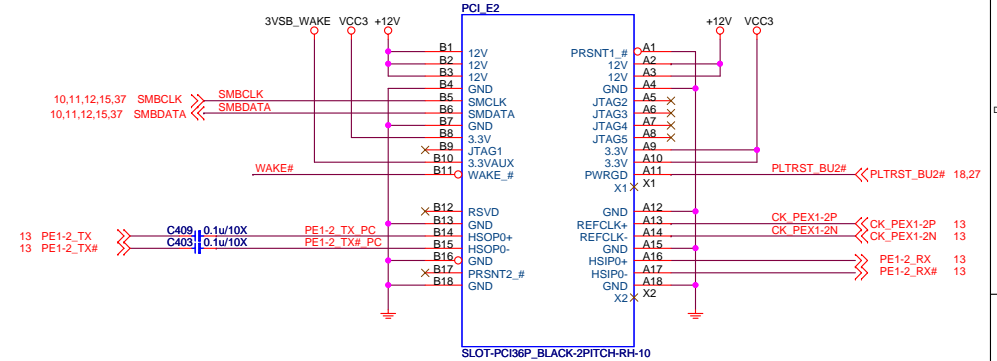
Date: Wednesday, May 26, 2010 Sheet 16 of 40



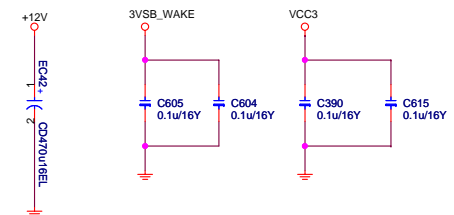
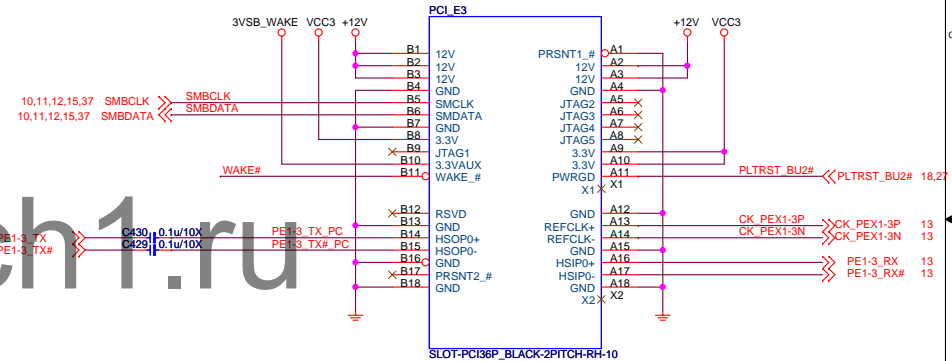
PCI_Express X16 Slot



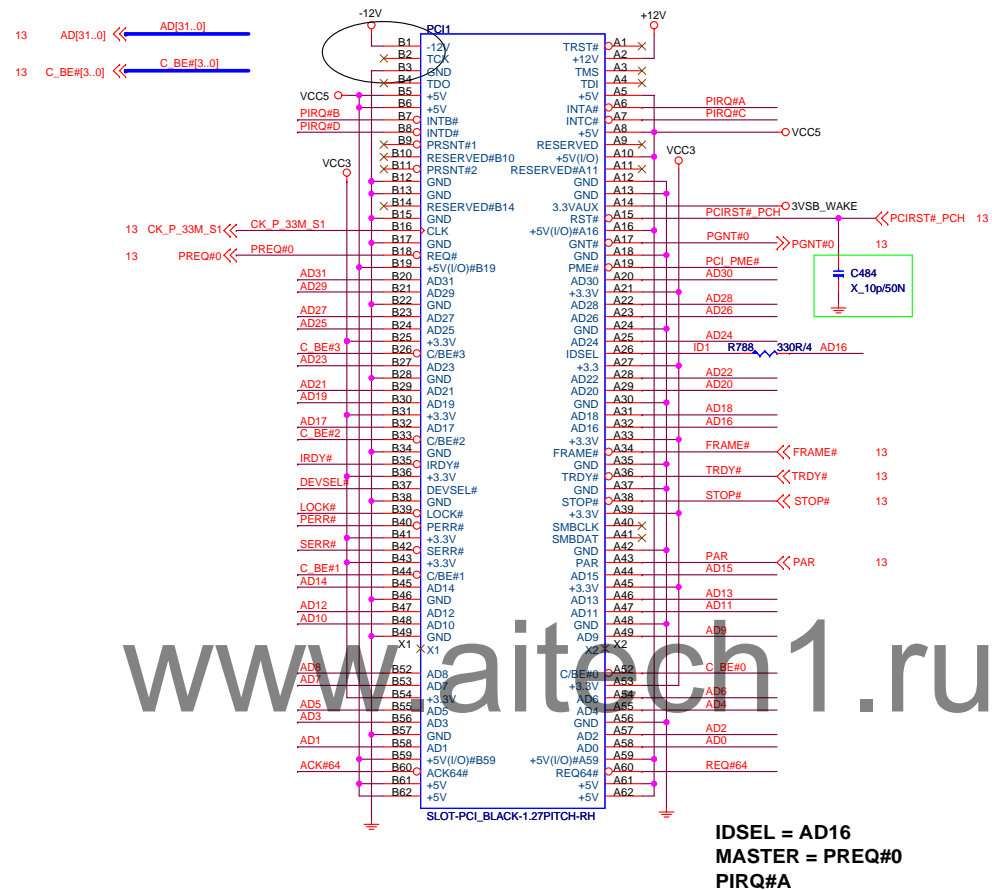
PCI EXPRESS x1-PORT2



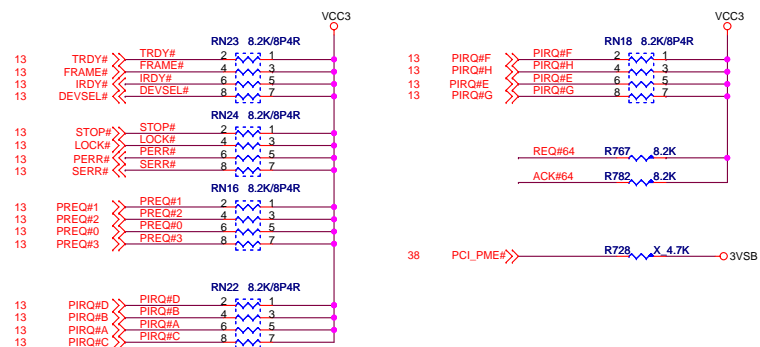
PCI EXPRESS x1-PORT3



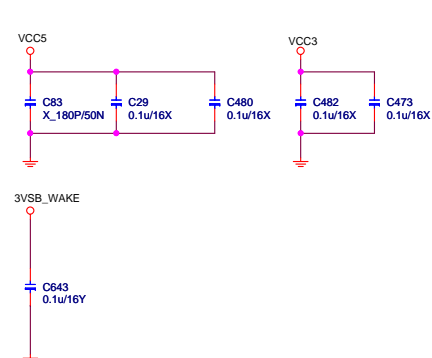
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

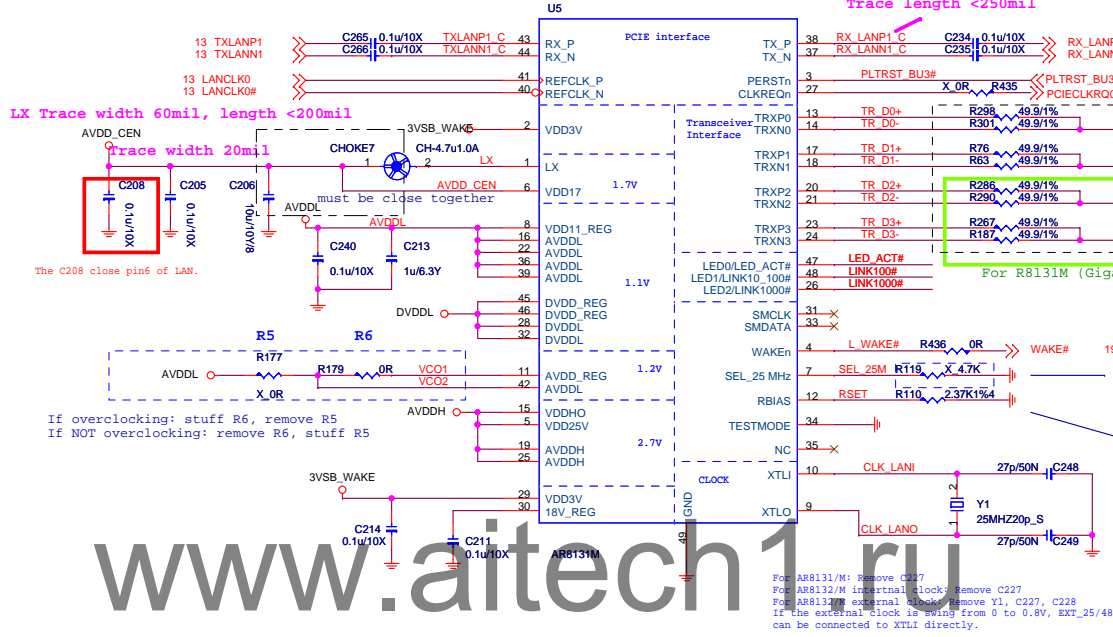
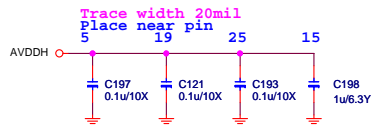
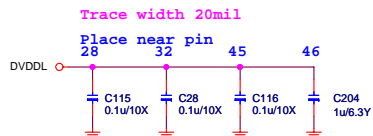
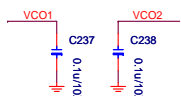
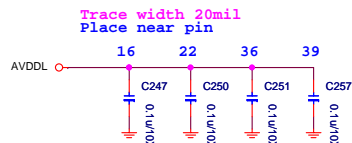
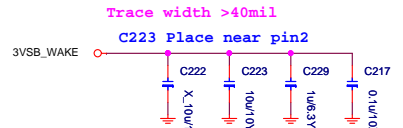


MICRO-STAR INT'L CO.,LTD

MS-7636

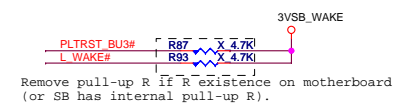
Size Custom	Document Description PCI Slot	Rev 2.0
Date: Wednesday, May 26, 2010		Sheet 20 of 40

AR8131M Giga & AR8132M 10/100M

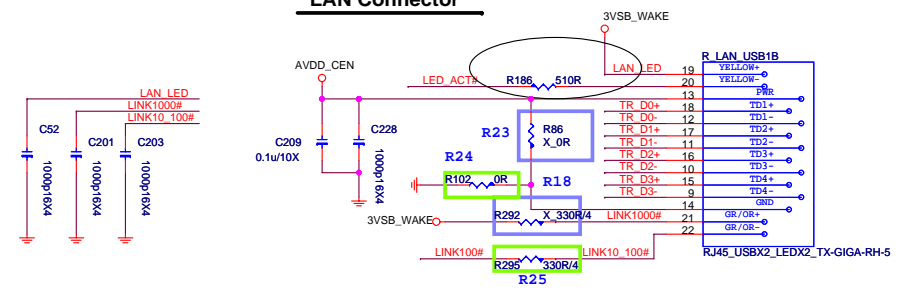


close to chip
1" < TR_Dx Trace length < 4"
differential impedance=100 ohm

The resistor should be placed as close to the LOM as possible.
The trace width keep about 10-15 miles.



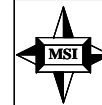
LAN Connector



R8131M (Giga):
remove R23, stuff R24
remove R18, stuff R25

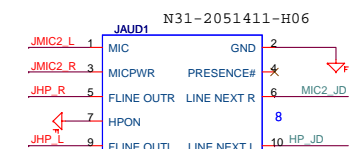
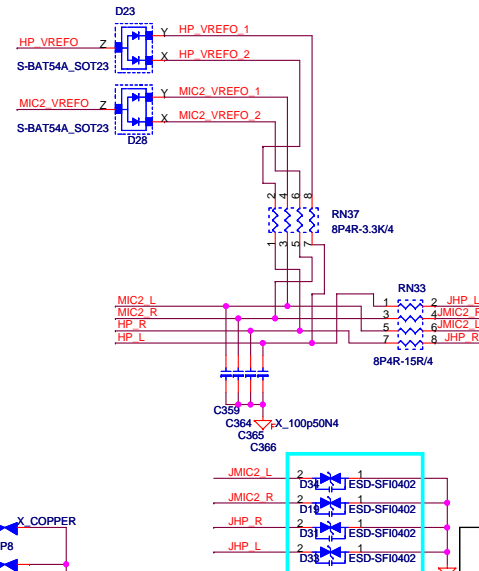
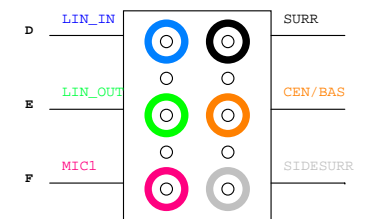
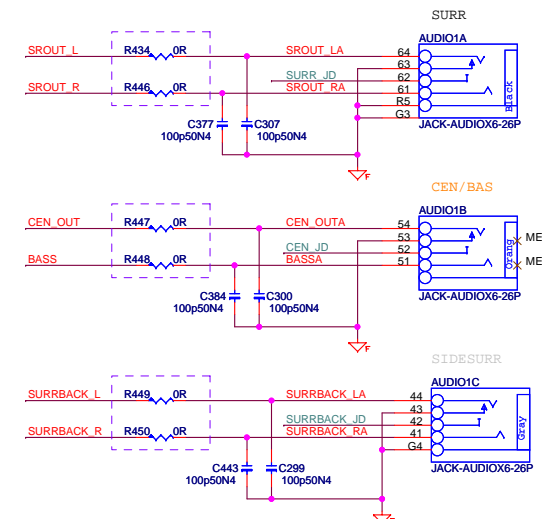
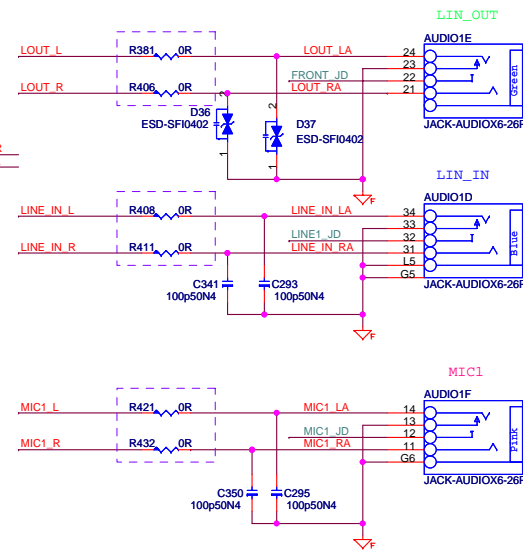
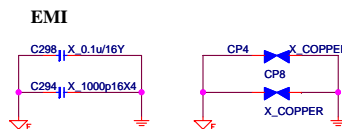
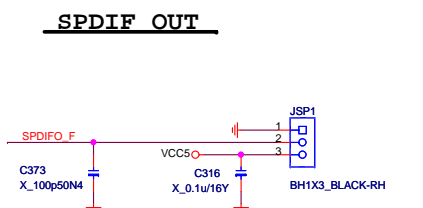
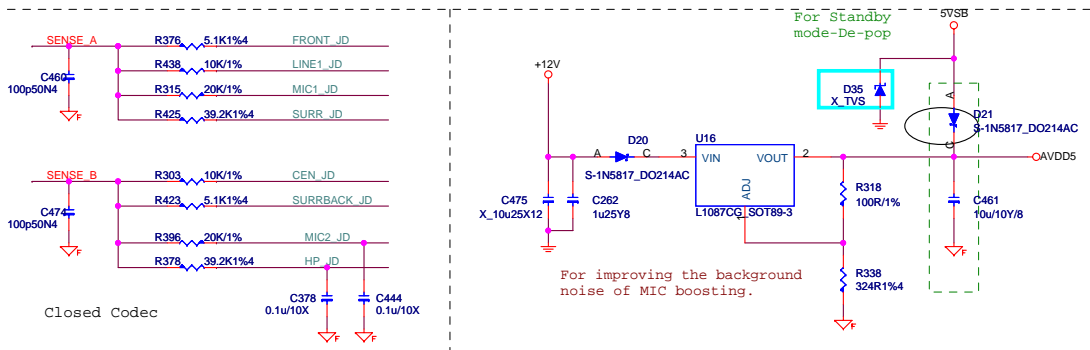
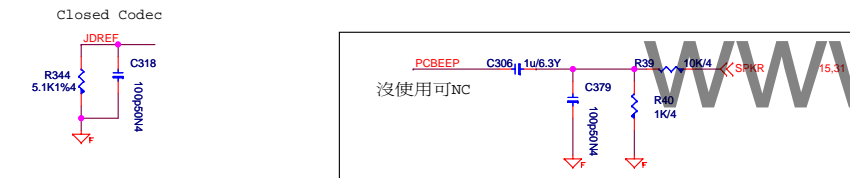
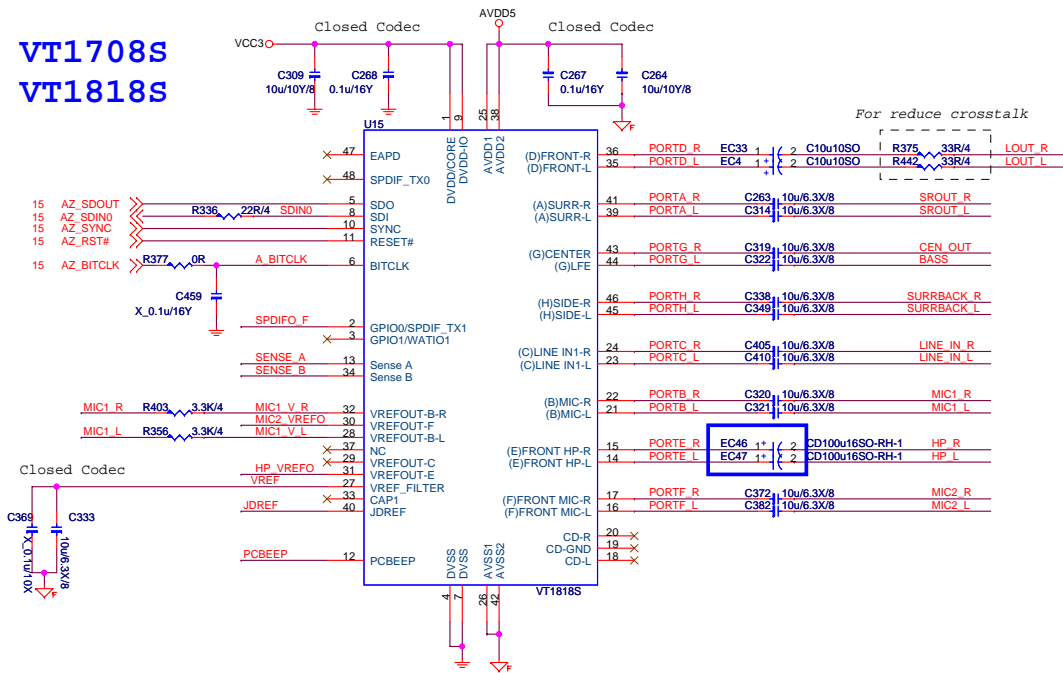
R8132M (10/100M):
stuff R23, remove R24
stuff R18

Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Orange
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22



MICRO-STAR INT'L CO.,LTD		
MS-7636		
Size	Document Description	Rev
Custom	AR8131M & AR8132M	2.0
Date: Wednesday, May 26, 2010	Sheet 21 of 40	

VT1708S
VT1818S



1828S與1708S線路相同
1828S performance較好，且有support Blue-ray



MICRO-STAR INT'L CO.,LTD			
MS-7636			
Size Custom	Document Description Audio Codec ALC889		Rev 2.0
Date: Wednesday, May 26, 2010		Sheet 22 of 40	

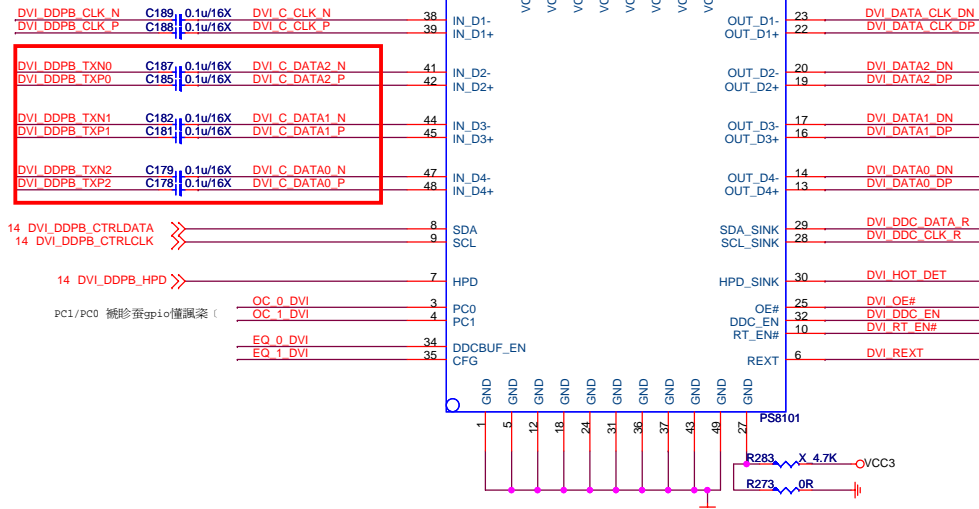
ESD protect
D0G-2950500-SI0
D0G-3010510-I05

DVI level shifter

14 DVI_DDPB_TXP0
14 DVI_DDPB_TXN0
14 DVI_DDPB_TXP1
14 DVI_DDPB_TXN1
14 DVI_DDPB_TXP2
14 DVI_DDPB_TXN2
14 DVI_DDPB_CLK_P
14 DVI_DDPB_CLK_N

PCH signal Mappings DG P156

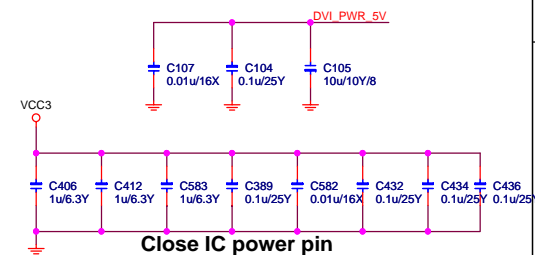
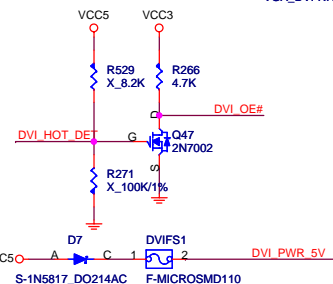
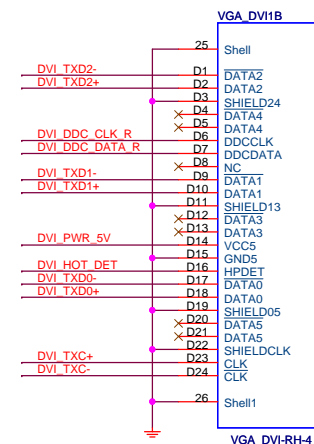
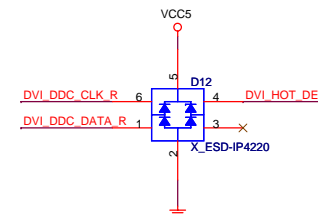
船廠郵路100ohm



PARADE料號:B0B-081010C-P97.

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reserve



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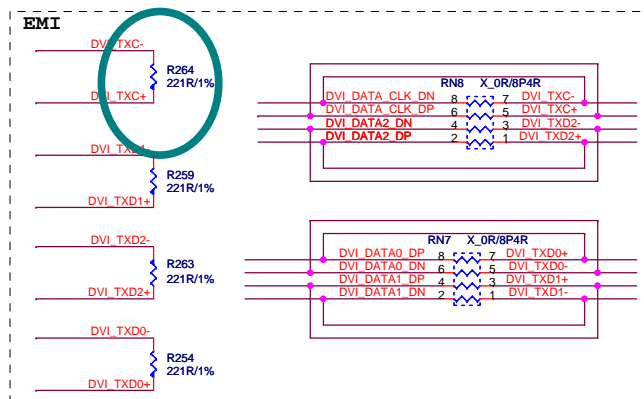
MS-7636

Size	Document Description	Rev
Custom	DVI transfer	2.0
Date: Wednesday, May 26, 2010		
Sheet 24 of 40		

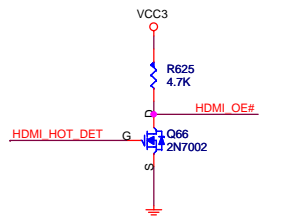
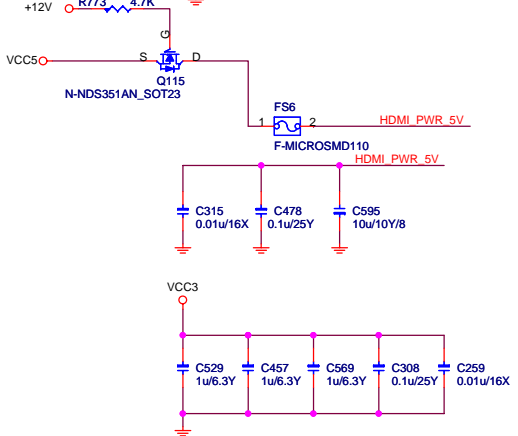
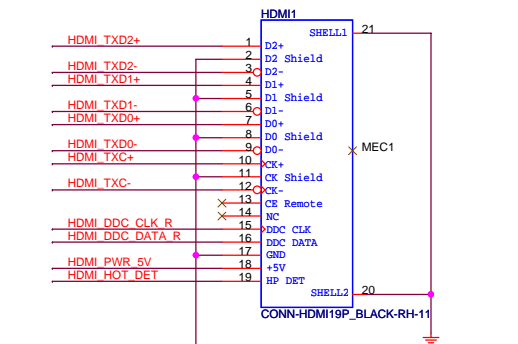
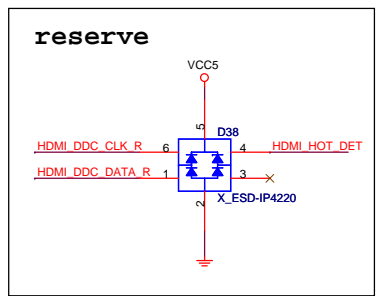
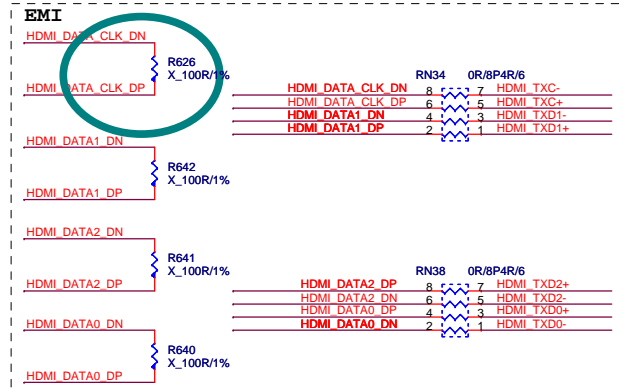
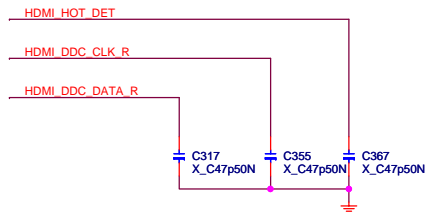
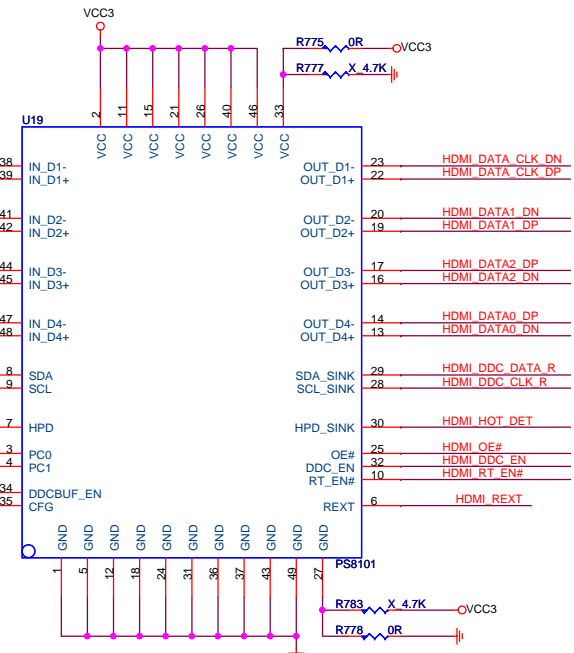
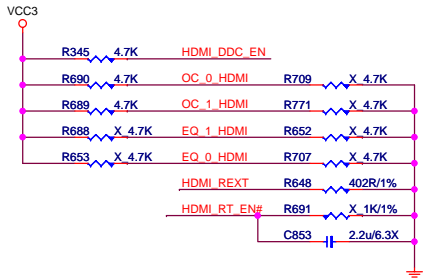
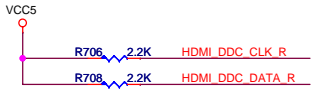
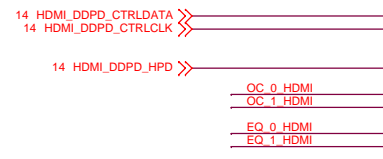
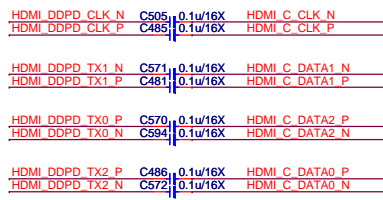
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm. The 4-dB equalization setting is recommended for PC motherboard level shifting to compensate PCB trace losses.
01	4 dB	
10	12 dB	
11	0 dB	



HDMI level shifter



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

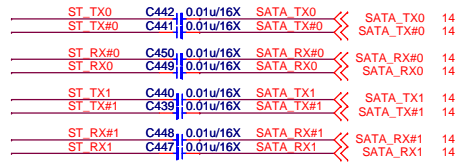
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

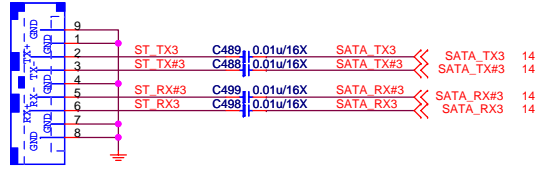
MICRO-STAR INT'L CO.,LTD
MS-7636
 Size Custom Document Description **HDMI** Rev 2.0
 Date: Wednesday, May 26, 2010 Sheet 25 of 40

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SATA connector (color:Black)

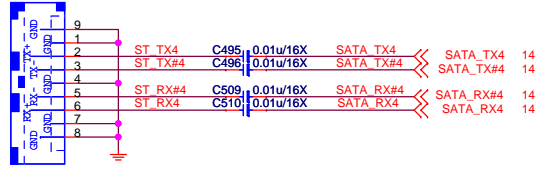


SATA4



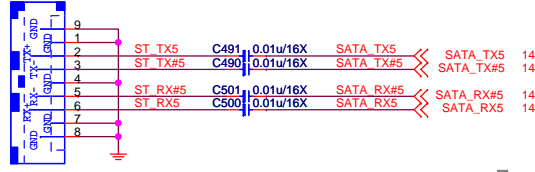
SATA7PM_BLACK-P-RH

SATA5



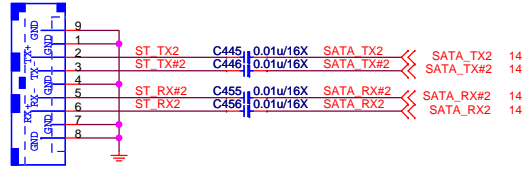
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SATA6



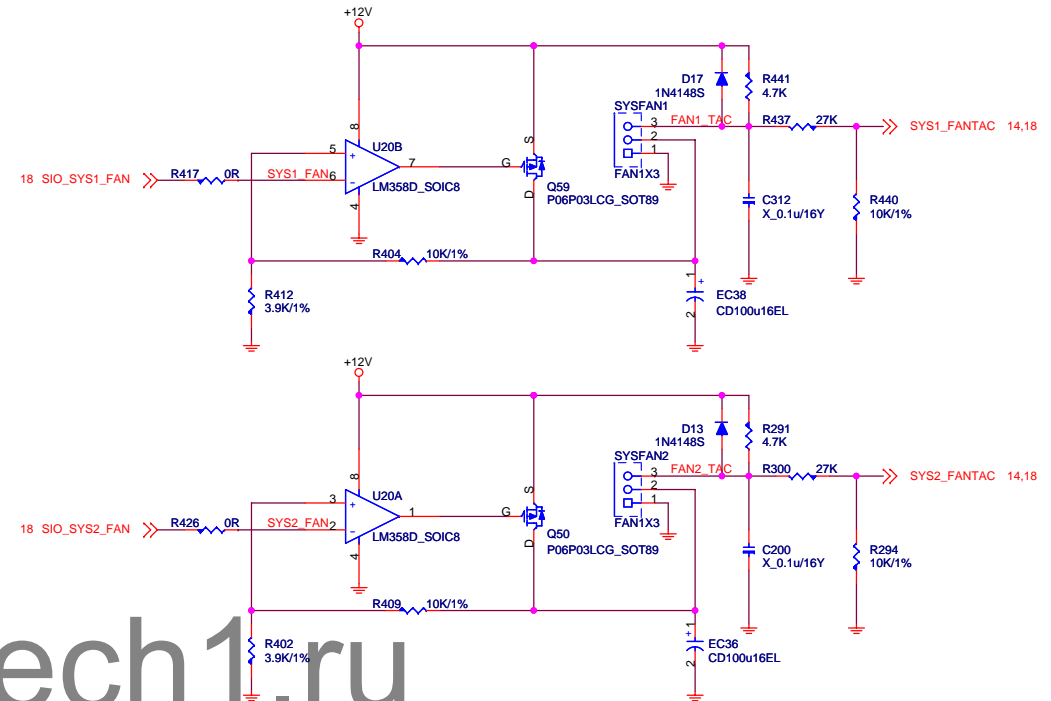
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SATA3

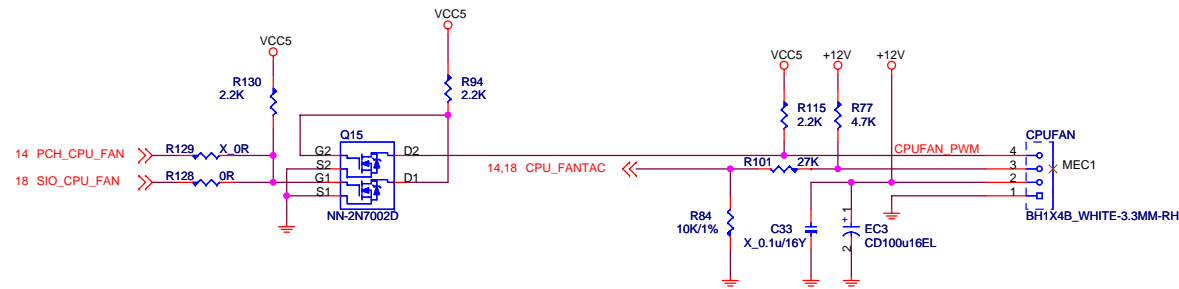


SATA7PM_BLACK-P-RH

FAN-COUNTROL CIRCUIT



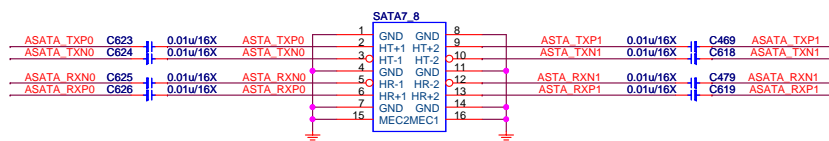
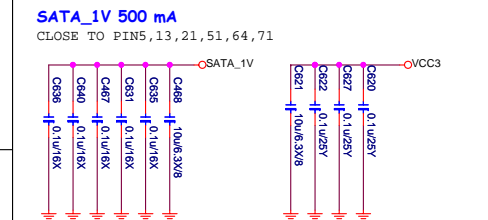
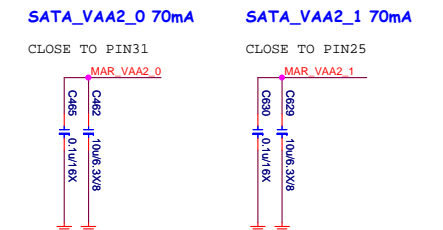
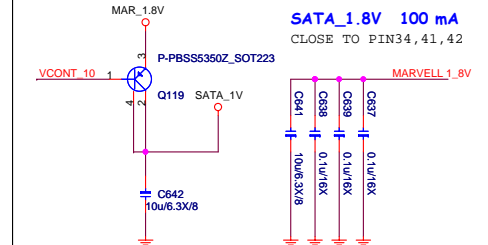
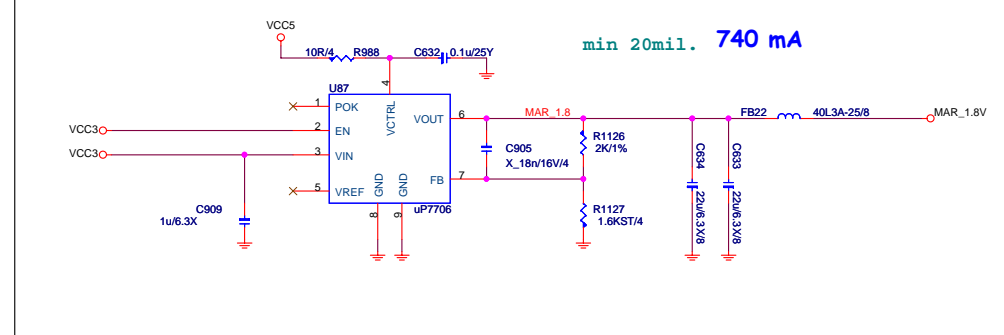
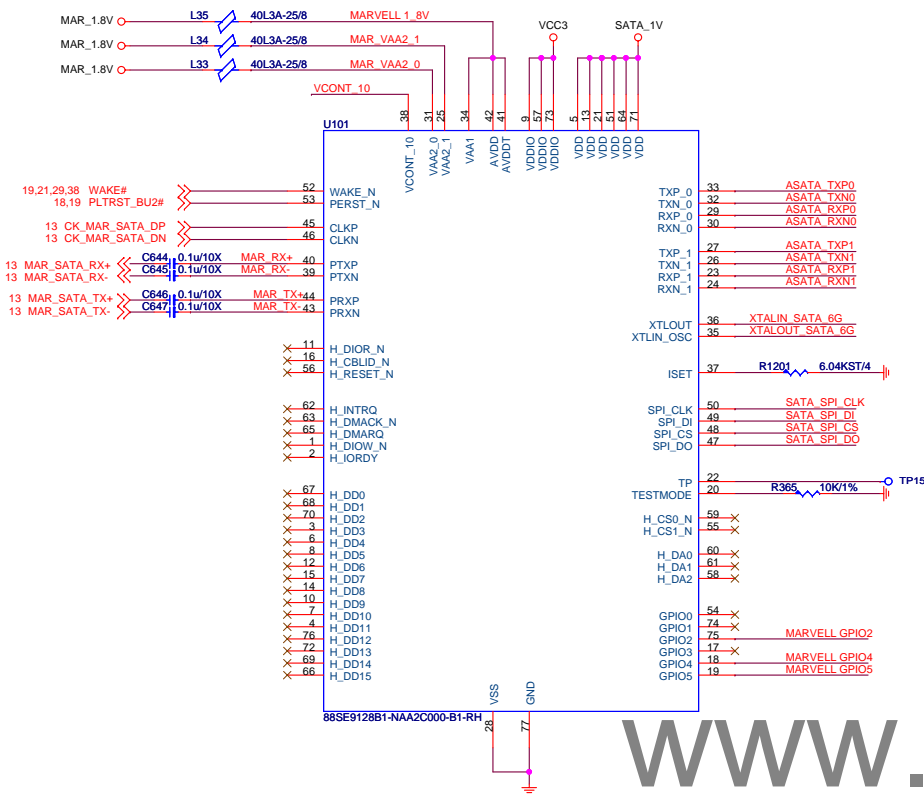
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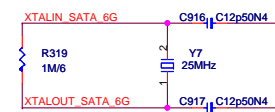
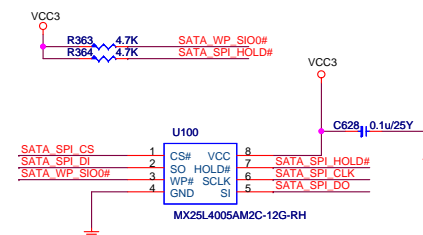
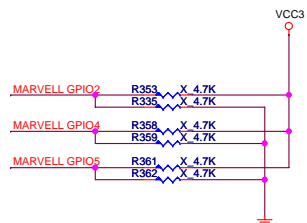
MICRO-STAR INT'L CO.,LTD

MS-7636

Size	Document Description	Rev
Custom	SATA & e-SATA Ports and Fan Control	2.0
Date: Wednesday, May 26, 2010	Sheet 26 of 40	

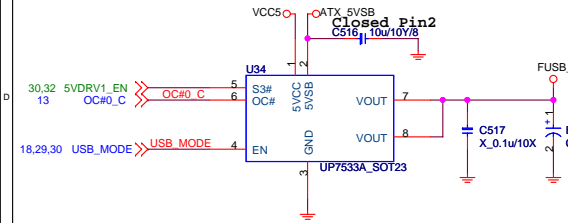


SATA14PM_BEIGE-ST-RH

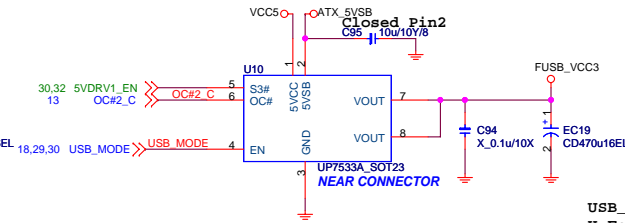


Rear USB Connector

USB POWER FOR PORT 0,1

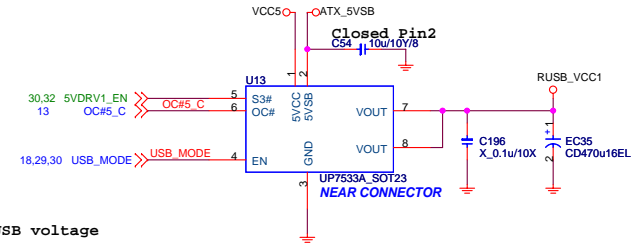


USB POWER FOR PORT 4,5

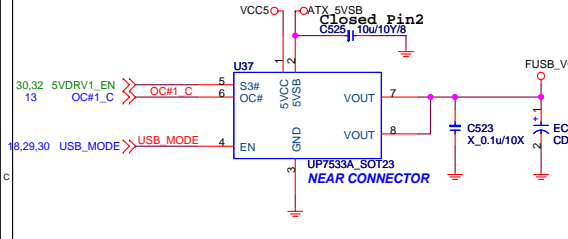


Front USB Connector

USB POWER FOR PORT 10,11

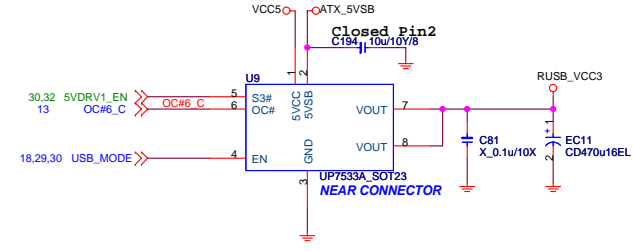


USB POWER REAL PORT 2,3

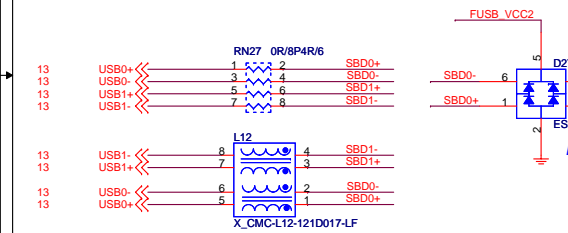


USB_MODE for USB voltage
H:Follow 5VSB
L:Always off

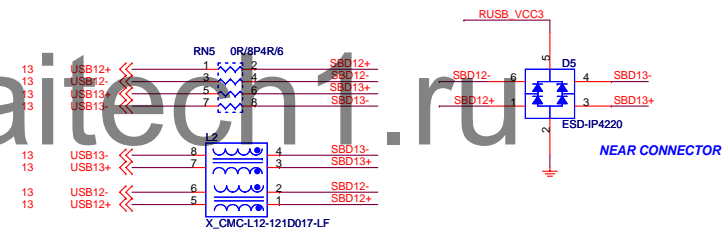
USB POWER FOR PORT 12,13



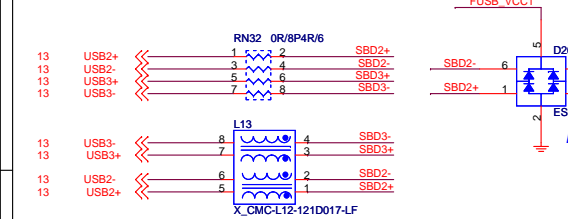
FRONT USB PORT 0,1



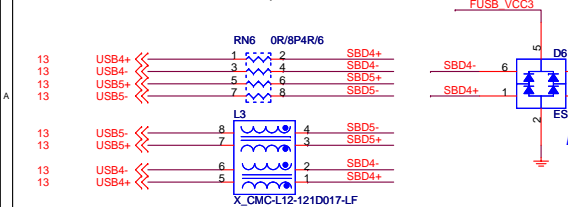
REAR USB PORT 12,13



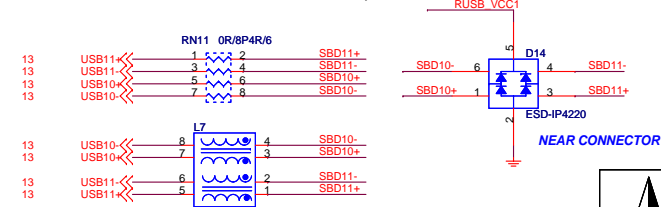
FRONT USB PORT 2,3

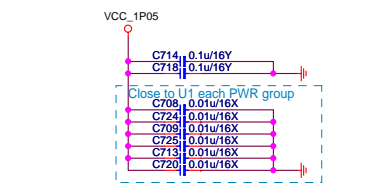
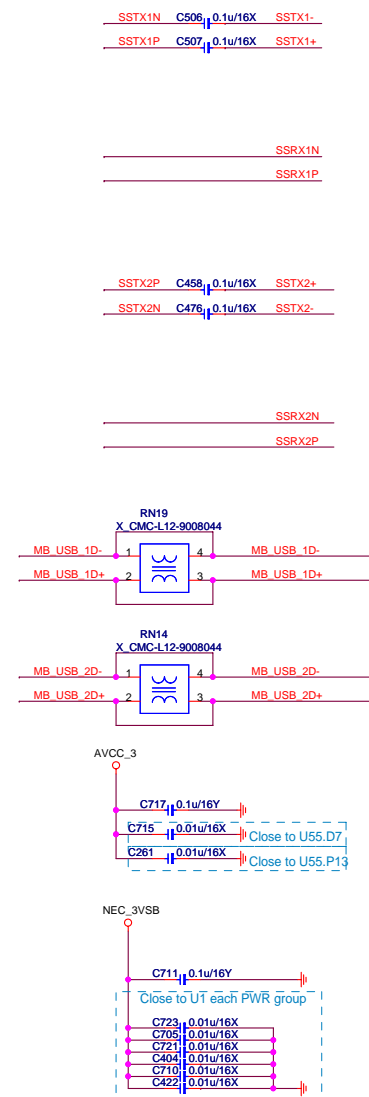
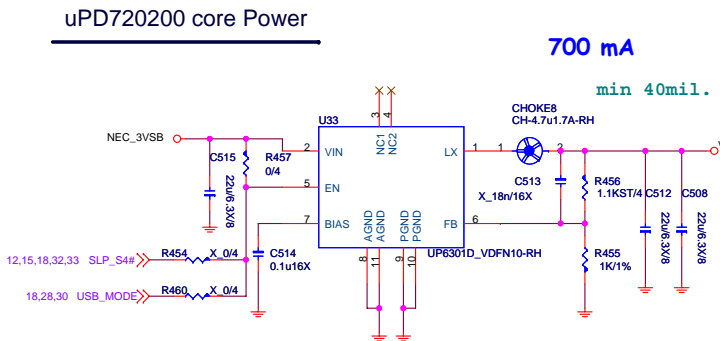
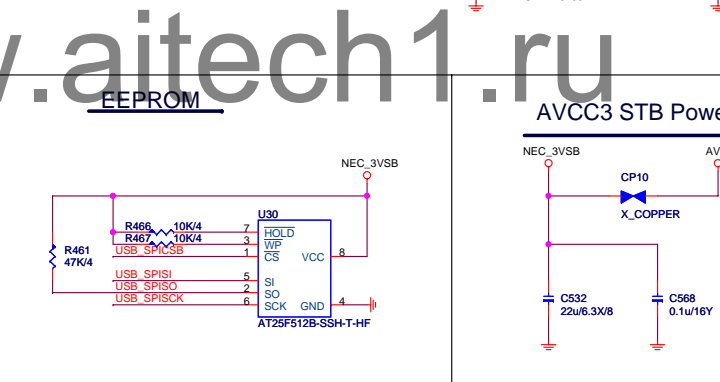
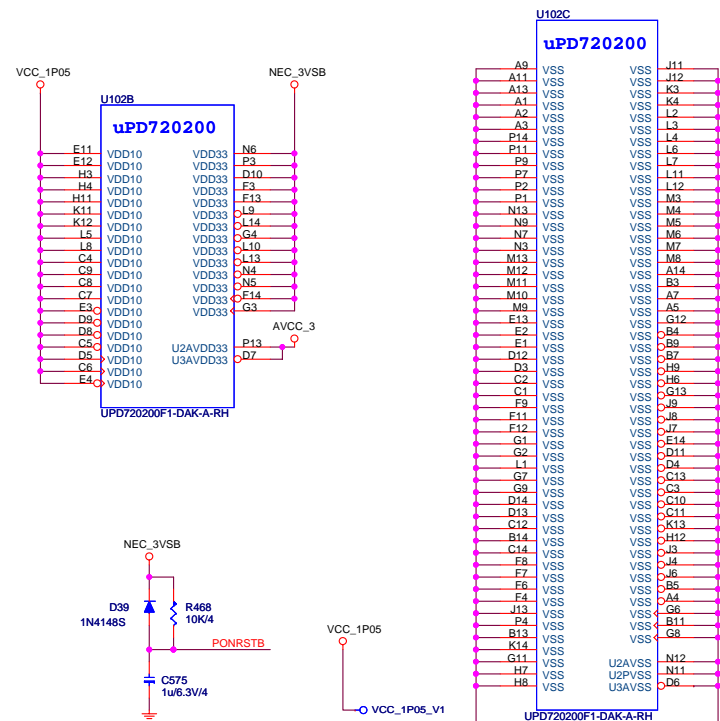
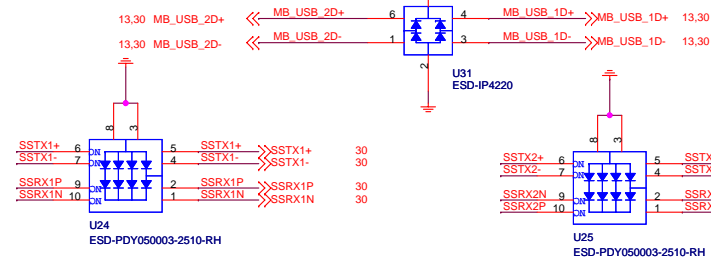


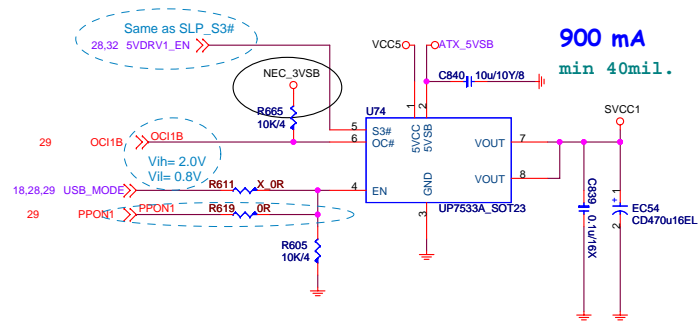
Front USB PORT 4,5



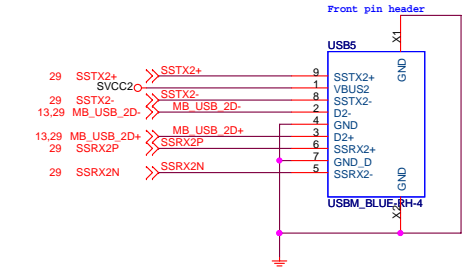
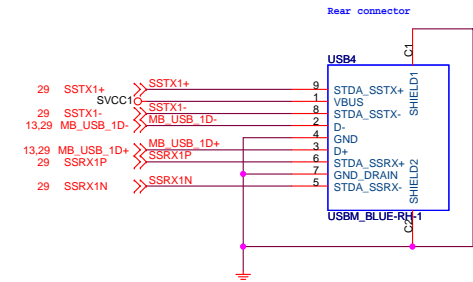
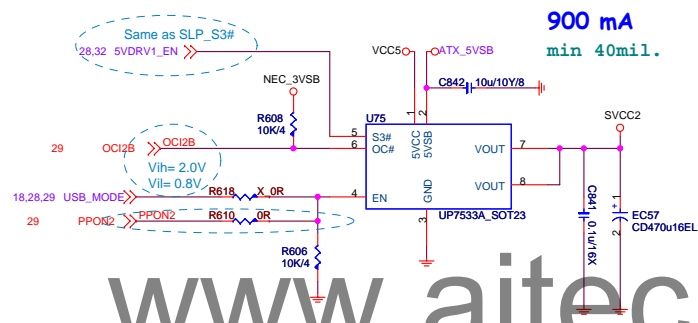
REAR USB PORT 8,9





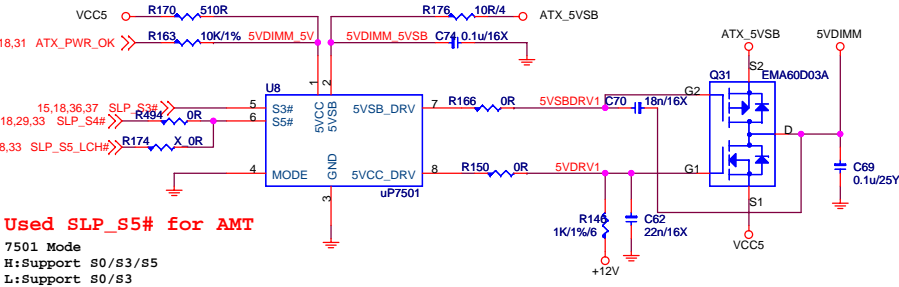


All power sources of uPD720200 are supplied, PPNx is enable.
PPONx is low when OCtx going to low.



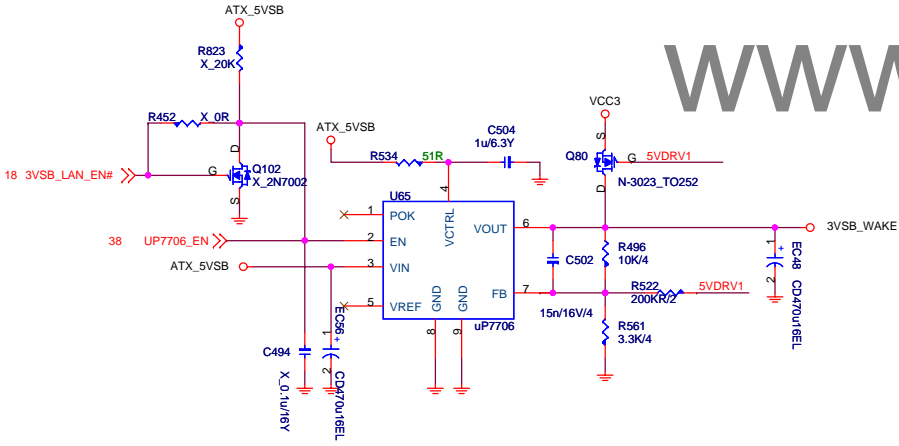
www.aitech1.ru

5VDIMM FOR DDR

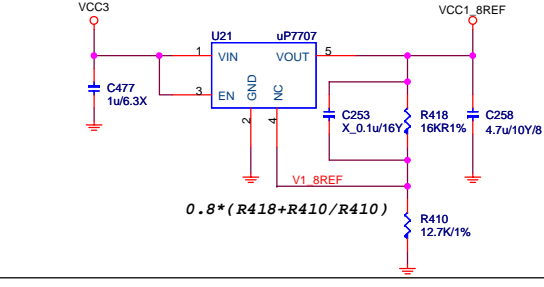


Used SLP_S5# for AMT
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

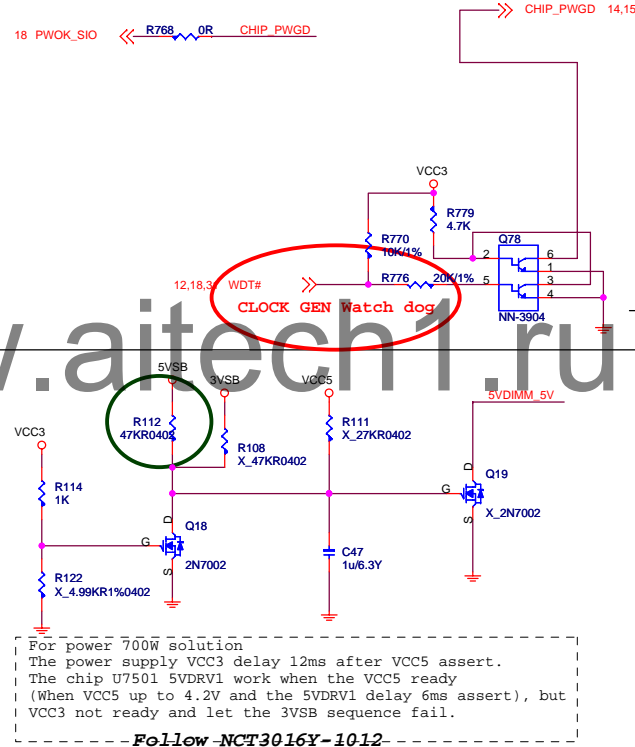
3VSB supply to PCH and other device.
Turn off when Deep S3/S5.
+3VSB_WAKE supply to PCI Slot and LAN power.
Turn off when Deep S3/S5 w/o WOL.



VCC1_8REF

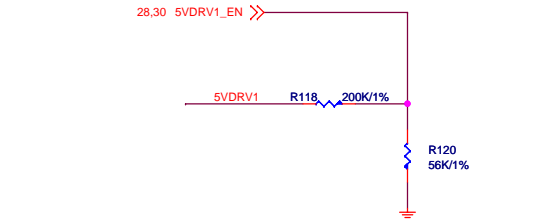


PWROK DELAY
VID before PWROK >3ms

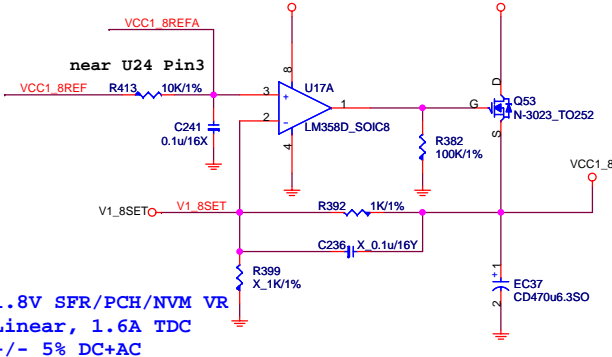


For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VSDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VSDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.
Follow NCT3016Y-1012

USB MODE

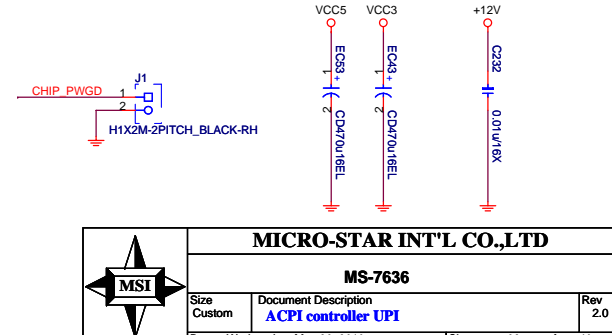
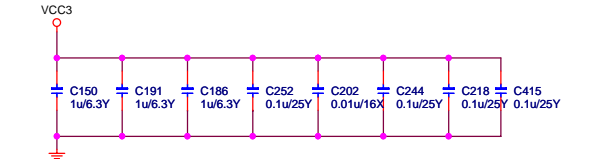
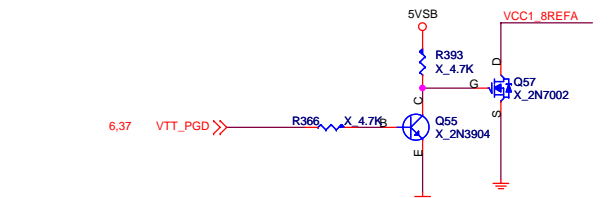


VCC1_8



1.8V SFR/PCH/NVM VR
Linear, 1.6A TDC
+/- 5% DC+AC

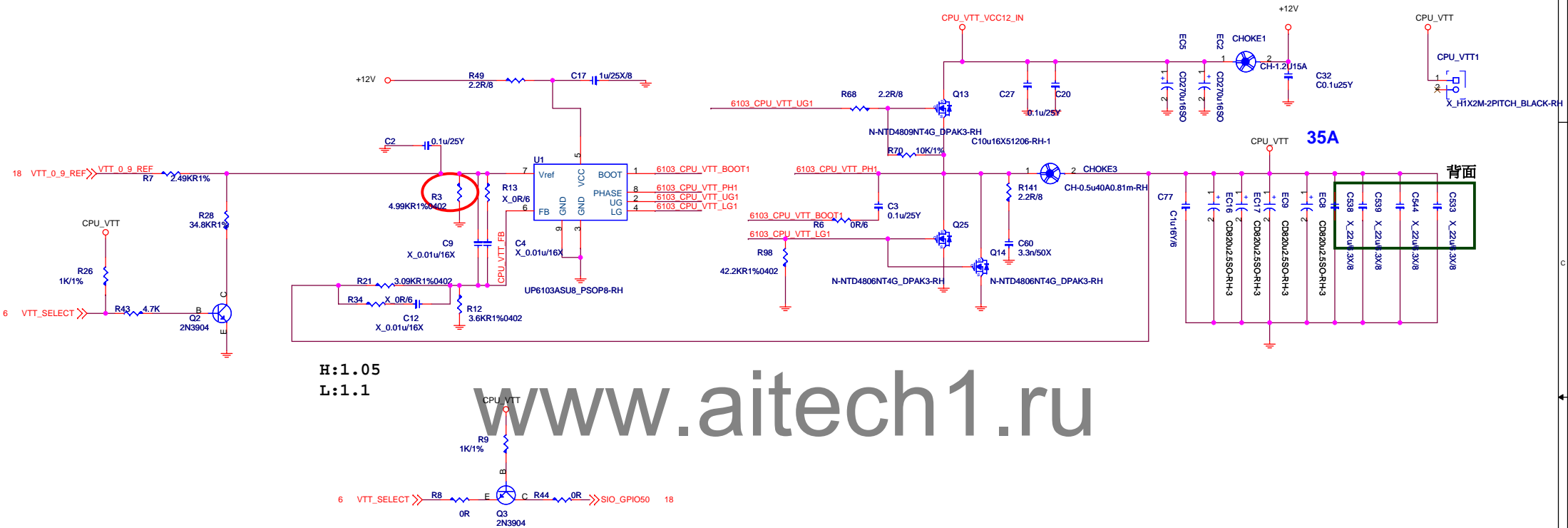
cpuvtt & pch vore wait 1.8v



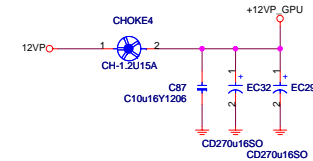
VTPWRGD LEVEL SHIFT

CPU_VTT
VTT0: 1.1V/1.05V CPU Uncore, MCP I/O

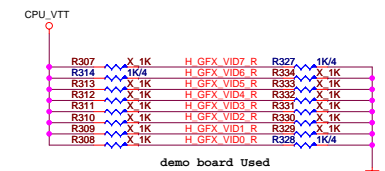
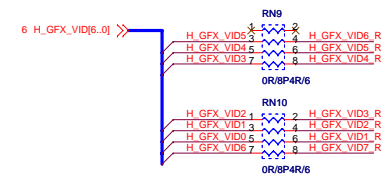
Irripple=8.28A
 $5.08 \times 2 \times 1 = 10.16A > 8.28A$



GFX 12V VIN



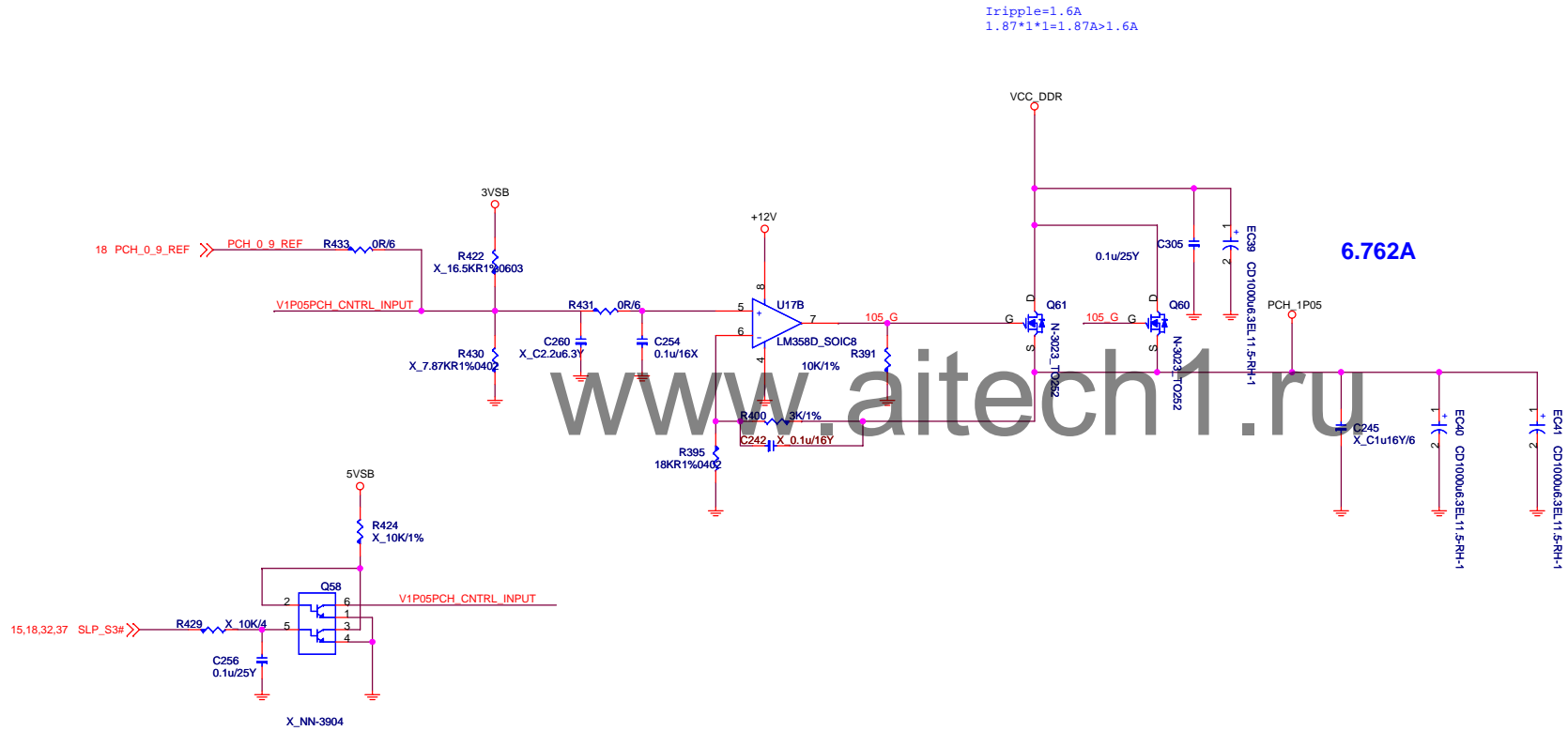
GFX 1PHASE OUTPUT



	MICRO-STAR INT'L CO.,LTD		
	MS-7636		
	Size Custom	Document Description GPU PowerISL6117_1-Phase	Rev 2.0
	Date: Wednesday, May 26, 2010	Sheet 35 of 40	

PCH Core 6.8A

**V1.05PCHS0: Vcc, VccExp, VccDMI, VccSATA,
VccSATAPLL, VccAUPLL, VccSSC, VccDIFFCLK,
VccDIFFCLKN, VccUSBCORE, VccDPLL, VccDPLL_EXP, VccDPLL_FDI (4.5A)
V1.05MEM: VccMEW, VccAUX, VccME (2.3A)**

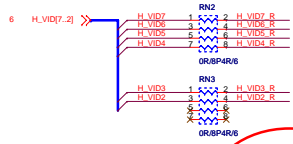


MICRO-STAR INT'L CO.,LTD

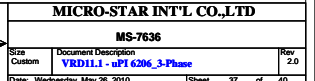
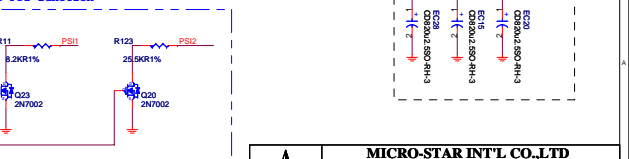
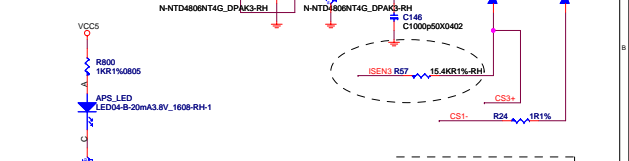
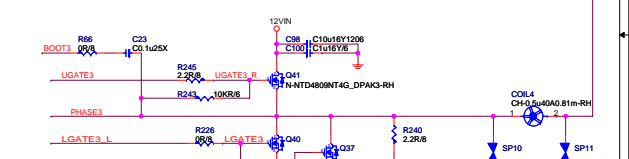
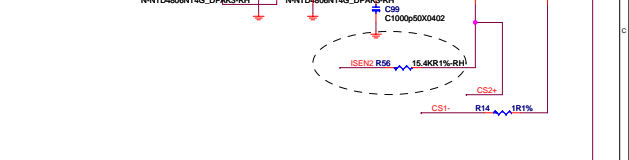
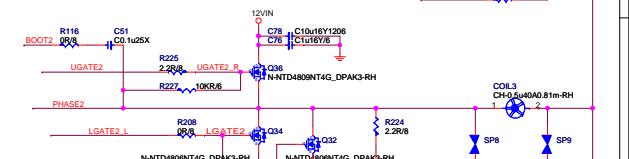
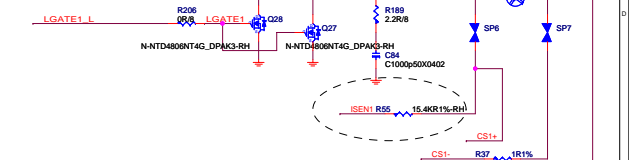
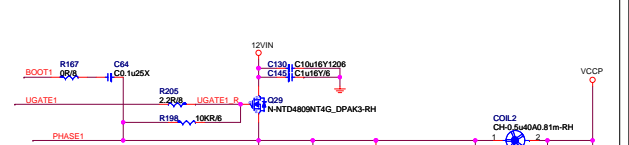
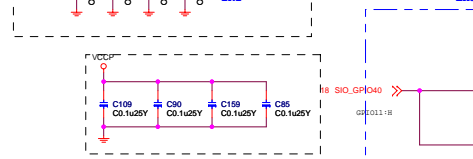
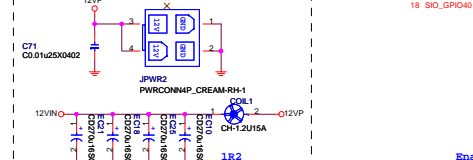
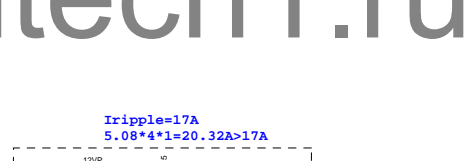
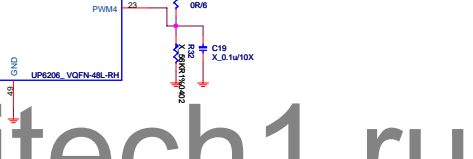
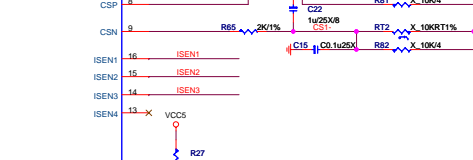
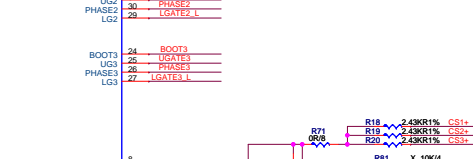
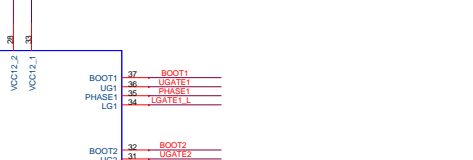
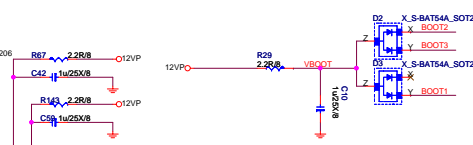
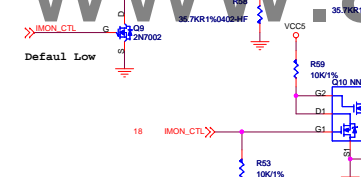
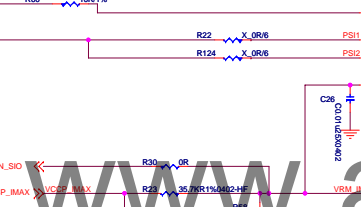
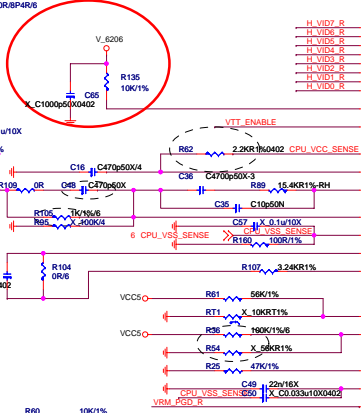
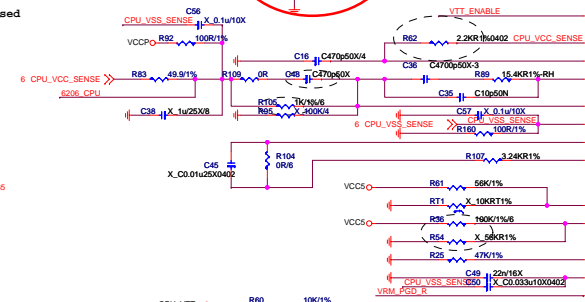
MS-7636

Size Custom	Document Description PCH POWER - UPI6103_1-Phase
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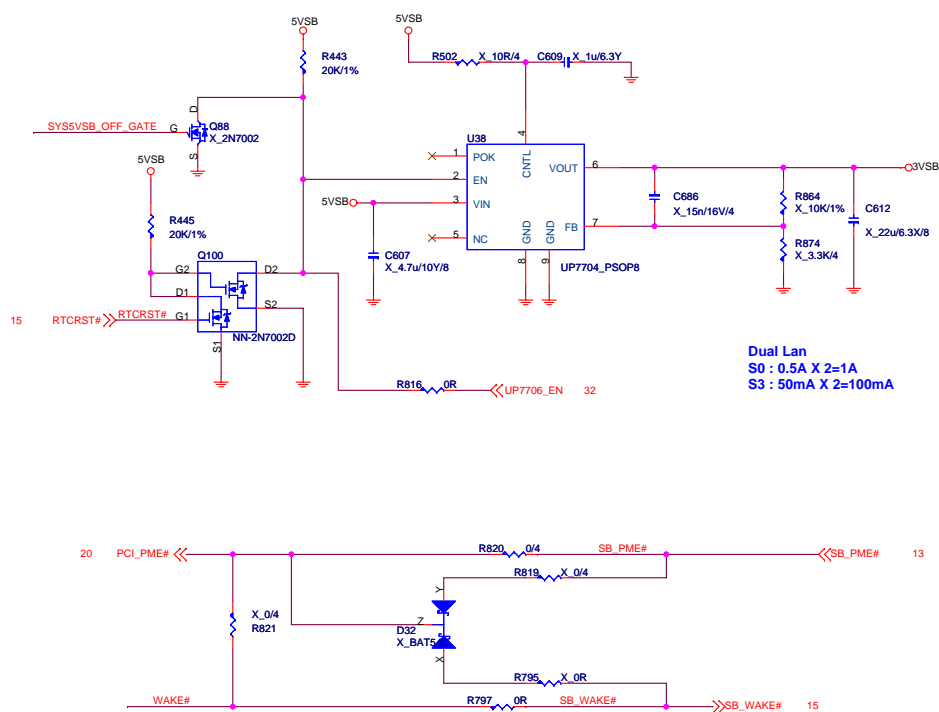
Date: Wednesday, May 26, 2010	Sheet 36 of 40
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[illegible]

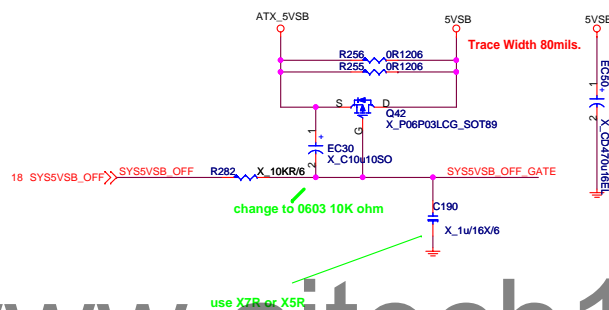
0x60:RH=10K,RL=NC



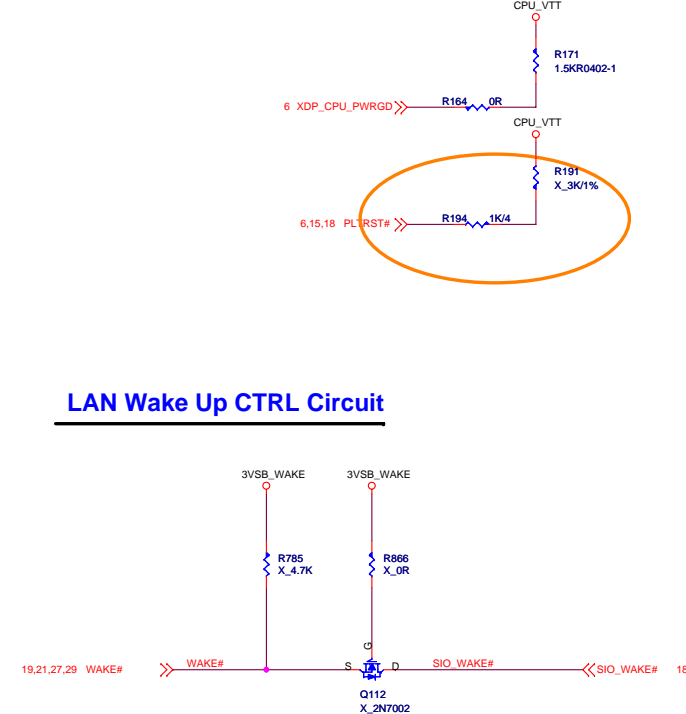
Deep Mode WOL LAN Power CTRL Circuit



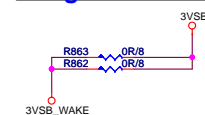
5VSB Power Switch



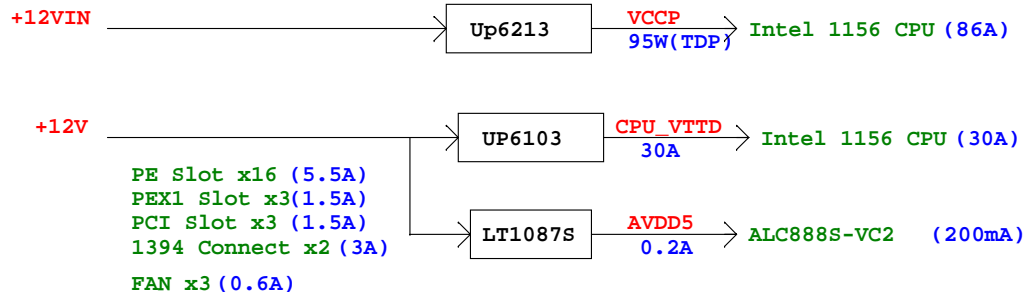
LAN Wake Up CTRL Circuit



Original LAN Power Source

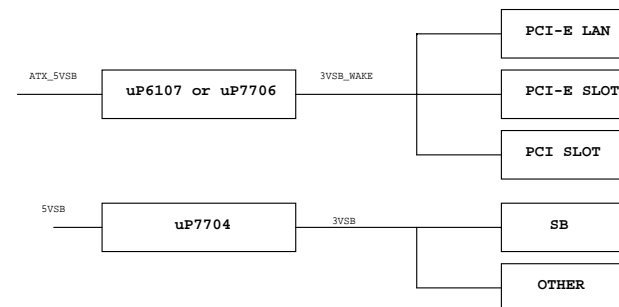


Dual Lan
S0 : 0.5A X 2=1A
S3 : 50mA X 2=100mA

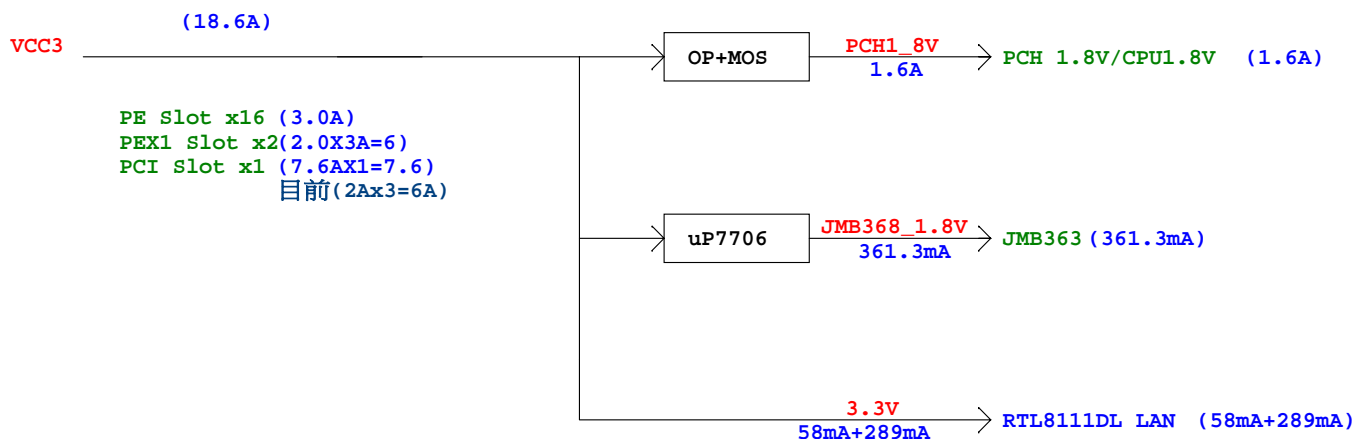
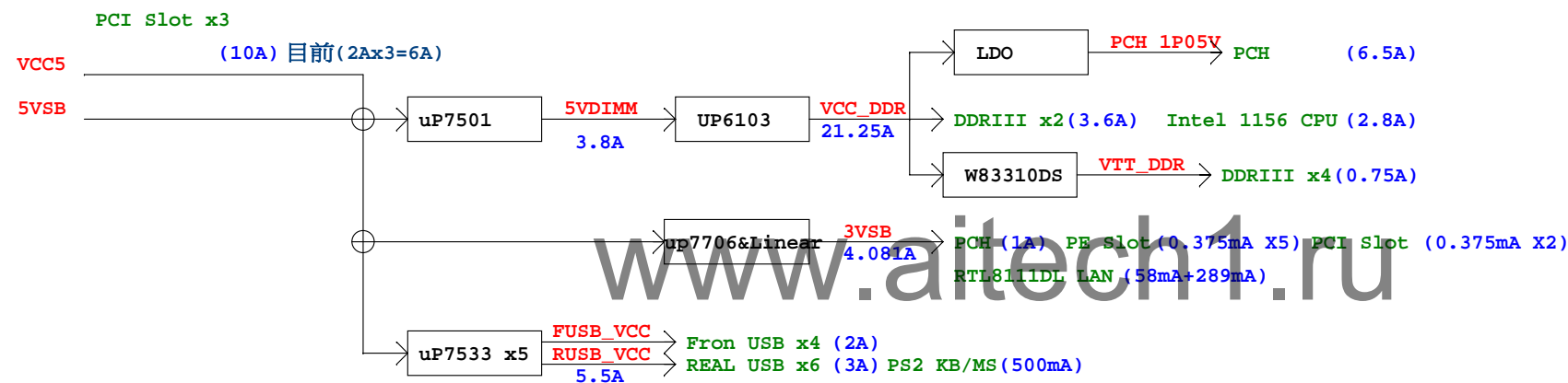


3VSB and 3VSB_WAKE POWER MAP

Add- 2009.9.28



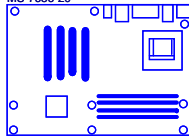
Power Delivery



MICRO-STAR INT'L CO.,LTD			
MS-7636			
Size	Document Description		Rev
Custom	Power Map		2.0
Date: Wednesday, May 26, 2010		Sheet	39 of 40

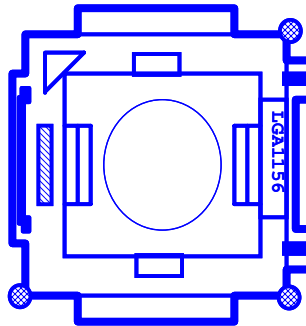
PCB

PCB1
<HP-BOM>
MS-7636-20

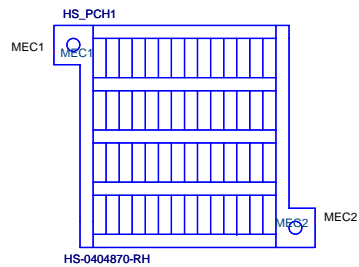


CPU SOCKET

XU1_X1
<HP-BOM>
CPU SOCKET



HEATPIPE



BATTERY

BAT1_X1
BAT-5CR2032P-RH



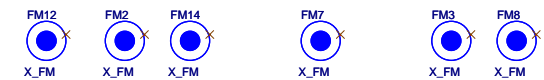
Rubber1
PCB
rubber

Rubber2
PCB
rubber

Simulation



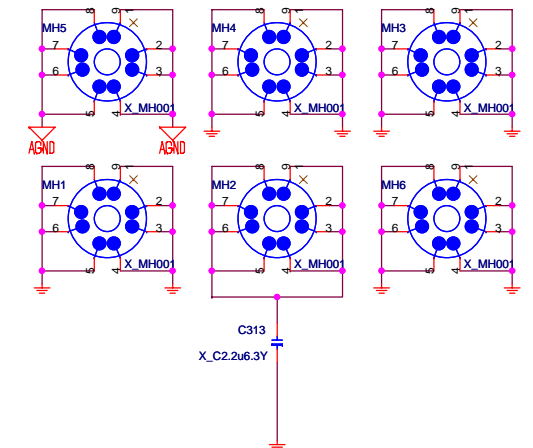
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



C313
X_C2.2u6.3V



MICRO-STAR INT'L CO.,LTD

MS-7636

Size
Custom

Document Description
Manual & Option parts

Rev
2.0

Date: Wednesday, May 26, 2010

Sheet 40 of 40